Low Cost Computer Subsystem For The Solar Electric Propulsion Stage (SEPS)

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TABLE OF CONTENTS

Table of Contents (Cont)

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Table of Contents (Cont)

LIST OF ILLUSTRATIONS

LIST OF TABLES

INTRODUCTION 1

This study was performed by the International Business Machines (IBM) Corporation in Huntsville, Alabama for the George C. Marshall Space Flight Center under contract NAS8-30749.

The purpose of the study was (1) to define the recommended SEPS Computer System design using performance, reliability and cost as the primary design parameters and (2) to perform a breadboard demonstration of selected system design elements. Redundancy implementation was emphasized and the Hybrid Technology Computer (HTC) version of the Space Ultrareliable Modular Computer (SUMC) family was used as the basis for evaluation.

In 1972 and 1973, IBM performed two SEPS Computer System design studies (References 1 and 2). These studies, along with IBM's ongoing HTC development activities, provided the foundation for this study. In addition, the SEPS Phase B Concept Definition Study was being performed concurrently with this study. Maximum advantage was taken to utilize information developed in that study to enhance the results of this Low Cost study and to insure compatibility of SEPS Program Requirements.

Two major areas were addressed in this study:

1) Systems Engineering effort which consisted of developing computer software and interface requirements, performing a redundancy

management and reliability analysis, and defining a computer/I/O design. Sections 3, 4 and 5 and Appendices A and B of this report document this effort.

2) Construction of a SEPS fault tolerant memory breadboard and demonstration of its operation. See Appendix C for documentation of this effort.

The SEPS subsystem which contains the computer is called the Command Computer Subsystem (CCS) and consists of the computer, custom input/output (I/O) unit and tape recorder for mass storage of telemetry data. This study is concerned only with the design of the computer and I/O unit. However, the reliability analysis was performed for the complete CCS including the tape recorders. Data for the tape recorders was supplied to IBM by Rockwell International Corporation.

STUDY SUMMARY 2

A study summary chart is shown in Table 2-1. The chart compares the CCS design which was developed during this study with the previous CCS design (Reference 2). Figure 2-1 gives a top-level block diagram of the CCS.

A summary of major study results follows:

- The SEPS Low Cost Study effort was begun with a review of past SEPS reports produced by IBM and Rockwell International Corporation. The purpose of this effort was to update our familiarization with past studies and to identify SEPS subsystems requirements changes which might impact the CCS requirements or interface definition. Based on this review, it was concluded that because of the stringent SEPS reliability requirement the SEPS computer configuration would include a fault-tolerant memory (FTM).

- The SUMC has been baselined as the CCS computer. In particular, the Hybrid Technology Computer (HTC) version of the SUMC was chosen. Because of the advanced state of development of the HTC, a much higher confidence level in the computer design is possible now than in previous studies. The HTC is a developed machine which has been delivered to MSFC. Fault tolerant aspects of the HTC are in an advanced state of development and a breadboard of the fault-tolerant memory was fabricated as part of this study. Accurate estimates of component failure rates and piece-part counts have contributed to

Table 2-1. SEPS CCS Design Summary

CCS FUNCTION/PARAMETER	GOAL	CURRENT DESIGN	PREVIOUS DESIGN 1973 TECH	PREVIOUS DESIGN 1975 TECH	REMARKS
Memory Size (16-Bits)	Unspecified	24K (~50% Contingency)	16K (~50% Contingency)	Same	Current design includes 4K TM buffer
CPU Speed Requirement (KAPS)	Unspecified	<6	<5	Same	
Weight (Kg) (lb)	9.1 ≤ 20	16.5 36.3	6.6 14.5	3.9 8.7	Excludes tape rec.
Volume (m^3) (in^3)	Unspecified	0.020 1210	0.006 364	0.004 216	Excludes tape rec.
Size (cm) (in)	Unspecified	25.5x56x14 10x22x5.5	10x23x25.5 4x9x10	10x14x25.5 4x5.5x10	Excludes tape rec.
Average Power (watts)	≤ 40	42.4	23	9	Includes tape rec. and assumes power switching
Interface Requirements	Unspecified	IN / OUT DIG 38 / 61 DIS 151 / 273 ANA 210 / 0	IN / OUT ANA & DIG 198 / 2 DIS 95 / 188	Same	
Reliability	≥ 0.95000	0.95039	0.9715	Same	Current design includes tape recorder, 4K TM storage and RAU functions
Technology					
Memory	Unspecified	N-MOS-LSI	N-MOS-LSI	CMOS-LSI	
Logic	Unspecified	TTL-LSI	TTL-MSI	CMOS-LSI	
Computer					
CPU Data Flow	Unspecified	16-bit	8-bit	Same	
Avg Processing Speed (KOPS)	Unspecified	~250	~100	Same	
Instruction Set	Unspecified	S/360	TC2	Same	
Instruction Length	Unspecified	16/32/48	16	Same	
Data Word Length	Unspecified	16/32/64	16/32	Same	
Input Power	30 ± 0.3 VDC	Nominal 28 VDC unregulated	Nominal 28 VDC unregulated	Same	
Thermal					
Operating (°C)	Unspecified	-55° to +80°	-55° to +80°	Same	
Standby (°C)	Unspecified	-55° to +125°	-55° to +125°	Same	

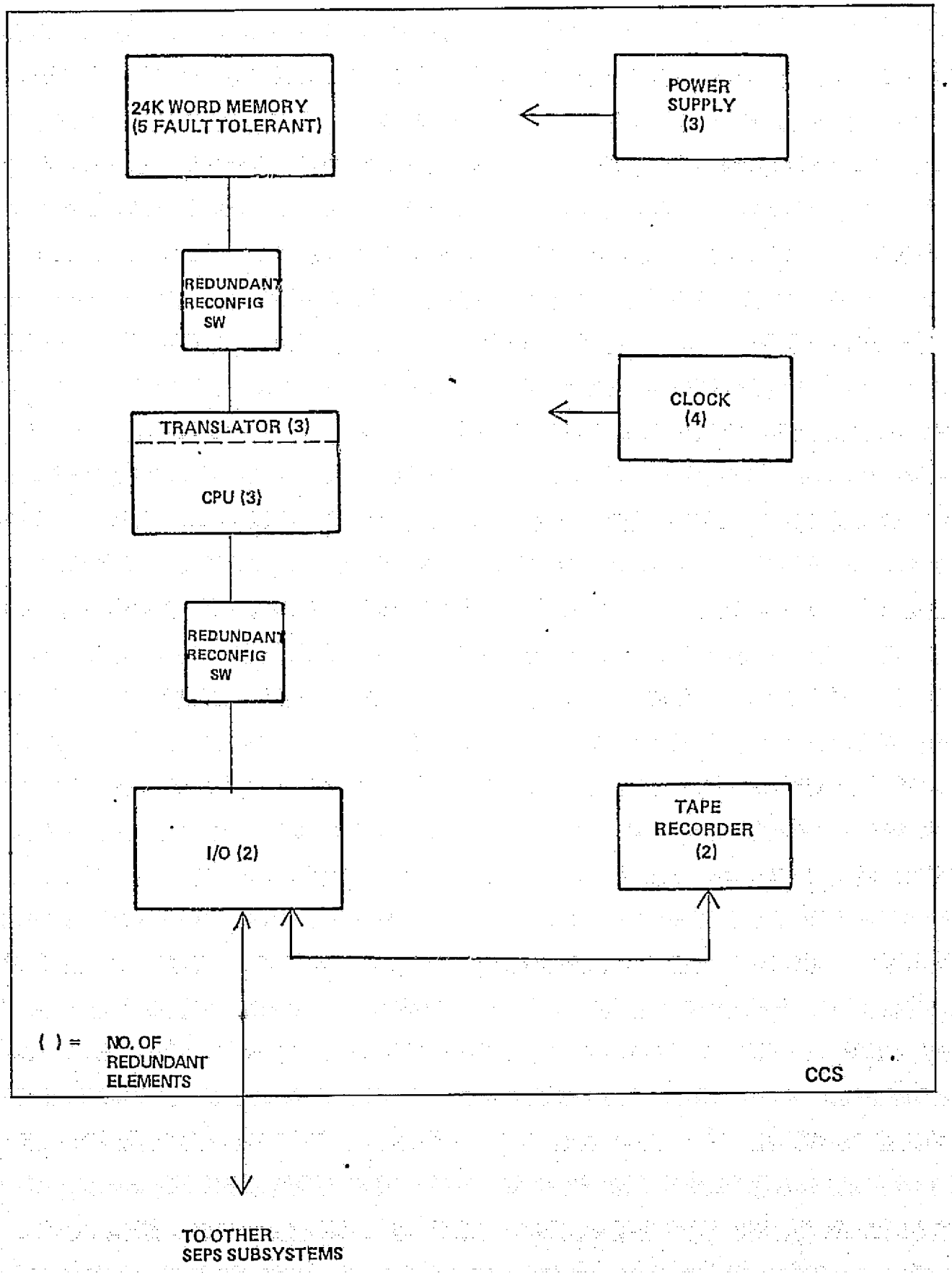


Figure 2-1. SEPS CCS Summary Block Diagram

increased confidence in the reliability and redundancy management analysis performed during this study. (Reference Section 4.2.2).

- A requirements analysis was performed which emphasized CCS signal interface definition and refinement of the previous software sizing study. Through coordinated efforts with the SEPS Phase B Study concurrently being conducted, a detailed list of interface signals and characteristics was developed. The baseline computer memory is 24K of 16-bit words. This includes 4K of telemetry data storage and approximately 50% contingency. (Reference Section 3).

- One of the major tasks of this study was to define the redundant custom I/O design. Emphasis was placed upon defining I/O hardware to interface the CCS with other SEPS subsystems. A trade study was performed which resulted in incorporating into the custom I/O most of the functions which had been previously performed by Remote Acquisition Units (RAU). (Reference Section 4.2.3).

- A reliability and redundancy management analysis was performed using updated study groundrules. The advanced state of development of the HTC also permitted more accurate estimates of component failure rates and piece-part counts. The CCS reliability goal of 0.95 for a three-year, unmaintained mission was met. This was accomplished considering the additional impacts of (1) an increased memory size,

(2) additional equipment in the I/O to perform most of the RAU functions, and (3) inclusion of tape recorders as a part of the CCS. (Reference Section 5).

- Additional trade studies were performed which contributed to the CCS baseline definition. Results of these studies are:

  - Incorporate 4K 16-bit word telemetry data storage in main memory rather than having a separate redundant buffer storage (Reference Section 4.2.4).

  - Adopt the centralized data acquisition concept within the custom I/O rather than having several RAU's distributed throughout the SEPS vehicle. (Reference Section 4.2.3.2.1).

- Since the fault tolerant memory is crucial to meeting the SEPS reliability goal, it was chosen as the computer system element which would be breadboarded. (Reference Appendix C).

CCS REQUIREMENTS 3

This section contains an updated electrical interface definition and an updated estimate of the onboard software requirements in terms of memory capacity and computer speed. The study reflects changes which have occurred in the SEPS study groundrules and SEPS subsystem design since the previous study (Reference 2) was completed. The major assumptions which impact requirements definition are listed below:

- Signal conditioning and formatting is done by the CCS for all subsystems except the solar array and propulsion subsystems
- Ten ion engines are baseline
- Eight power processors are baseline
- Four Hg propellant tanks are baseline
- SEPS for planetary missions has 16 RCS thrusters and both hydrazine and krypton RCS propellant. SEPS for earth orbital missions has 26 RCS thrusters using hydrazine
- SEPS for planetary missions has high gain communication antenna, an X-band and S-band system. SEPS for earth orbital missions has TV system
- Interface between the CCS and each power processor in the propulsion subsystem consists of one serial digital channel for sending commands and for receiving status data
- Local remote acquisition units are located at the solar array wings to convert and multiplex solar array current, voltage and temperature measurements.

3.1 INTERFACE DEFINITION

Early in the study an effort was undertaken to define detailed CCS signal interface data. The result of this effort is shown in summary form in Table 3-1, and detailed interface definition is given in Appendix A.

Generally, the interface requirements increased from the previous study. More emphasis was placed on interface definition during this study and more detail was available for other subsystems. The data developed in this section was used in defining the custom I/O design (Reference Section 4.2.3).

3.2 SOFTWARE SIZING

A thorough software sizing review was conducted of the two previous studies which IBM performed (References 1 and 2). This review along with coordinated effort with the SEPS Phase B study concurrently being conducted permitted an updated software sizing to be developed.

3.2.1 MAJOR CHANGES

Below is a summary of the major baseline software sizing changes from the data developed in Reference 2. Comments are applicable to both SEPS planetary and earth orbital missions unless otherwise indicated. Table 3-2 summarizes the changes.

3.2.1.1 Memory Capacity

Total memory storage capacity requirements decreased by approximately 6% for SEPS planetary missions and increased by approximately 6% for SEPS earth

Table 3-1. SEPS CCS Interface Requirements Summary

	CCS OUTPUTS			CCS INPUTS		
	DIG	DIS	ANALOG	DIG	DIS	ANALOG
Guid., Nav. & Att. Control	20	58(84)	0	12	32(46)	86(107)
Propulsion	8	52	0	0	40	16
Communications	8(4)	14(13)	0	3	0	31(28)
CCS/DHS	3(6)	12	0	0	4	4
Solar Array	4	10	0	2	12	2
Structures & Mechanisms	2(0)	70	0	2(0)	26(22)	15
Thermal Control	0	0	0	0	0	0
Power Distribution	0	18	0	0	19	27
*Attached Science Package	16(0)	39(0)	0	19(0)	18(0)	29(0)
TOTALS	61(42)	273(259)	0	(17)	151(143)	210(199)

*Planetary missions only

NOTE: When Earth Orbital mission interfaces are different from Planetary mission interfaces, Earth Orbital interface requirements are enclosed in parentheses.

Table 3-2. SEPS Software Sizing Summary

	PLANETARY				EARTH ORBITAL			
	WAS		IS		WAS		IS	
	MEMORY	SPEED	MEMORY	SPEED	MEMORY	SPEED	MEMORY	SPEED
Executive	2175	0.72	2175	0.72	2175	0.72	2175	0.72
Propulsion	1476	0.92	1476	0.92	1476	0.92	1476	0.92
Attitude Control	4465	0.67	2483	0.81	4465	0.67	2688	0.85
Guidance & Navigation*	110	0.03	110	0.03	462	0.02	2097 (11097)	1.14 (2.50)
Data Handling**	485	0.13	742	0.14	485	0.13	765	0.14
Communications	1193	0.29	1934	0.47	1030	0.15	1386	0.24
Solar Array	180	0.15	180	0.15	180	0.15	180	0.15
Power Distribution	0	0	350	0.15	0	0	350	0.15
Mechanisms	107	0	105	0	127	0	125	0
Thermal	0	0	0	0	0	0	0	0
Redundancy Management	1795	1.31	1597	1.19	1945	1.31	1747 (2197)	1.29 (1.59)
Science Payload	0	0	200	0.01	--	--	--	--
	11986	4.22	11352	4.59	12345	4.07	12989 (22439)	5.60 (7.26)

*Includes Approach Guidance Sensor
**Does not include 4K telemetry data requirements
Memory sized in 16-bit words
Speed sized in thousands of equivalent add-operations per second (KAPS)
( ) Indicates high-autonomy G&N (Optional)

orbital missions excluding the 4K telemetry buffer which was added to main memory (Reference Section 4.2.4). Major items which contributed to these changes are given below.

Attitude Control

This software sizing decreased by nearly 50% reflecting the change from processing star mapper sensors to processing star tracker equipment.

Guidance & Navigation

This software module increased from approximately 500 words to approximately 2000 words for earth orbital missions, reflecting the requirement to perform more G&N functions onboard. Examples are: vehicle and target state propagation, laser radar processing for rendezvous, and rendezvous guidance.

Data Handling

The data handling function increased approximately 35% due to additional telemetry measurements to be processed.

Communications

Planetary mission sizing increased approximately 60% and earth orbital mission sizing increased approximately 40% due to the identification of additional ground commands which must be processed onboard.

Power Distribution

This is new software that has been sized for this study. Previously no software had been required for the control of equipment in this subsystem.

Redundancy Management

This software sizing had a net decrease of less than 10% due primarily to the addition of communications subsystem redundancy management and the decrease in data handling and electrical functions.

Science Payload

This is new software sizing that has been sized for this study to provide support to SEPS planetary mission payloads. Previous studies did not consider payload function logic.

3.2.1.2 CPU Speed

Total CPU speed requirements increased by approximately 9% and 38% for planetary and earth orbital missions, respectively. The major items which contributed to the increases are listed below.

Attitude Control

CPU speed requirements for this function increased about 20% due to the increase in the number of instructions required for attitude reference and TVC/RCS processing.

Guidance & Navigation

For earth orbital missions, the increase in the CPU speed requirements for this function accounted for almost all of the total change. Additional G&N functions were added to the baseline SEPS, with the vehicle state propagation execution rate accounting for most of the increase.

Communications

Additional commands which were added during this study caused an increase in the execution rate.

3.2.2 DETAILED SIZING DATA

Tables 3-3 and 3-4 give the summary software sizing requirements for the SEPS planetary and earth orbital missions, respectively. Appendix B gives the detailed software sizing requirements for the SEPS planetary and earth orbital missions. A description of each software function is given below. Comparisons are made with the previous study (Reference 2).

3.2.2.1 Executive

No changes are recommended to the Executive function sizing for either the planetary or earth orbital missions. See Page 6-14 of Reference 2 for a detailed description of the Executive function.

3.2.2.2 Propulsion

Contact was made with Hughes Research Laboratories (HRL) by Rockwell International. HRL recommended no sizing changes for this function. See Page 6-16 of Reference 2 and Page A-15 of Reference 1 for a detailed description of propulsion subsystem subtasks.

3.2.2.3 Attitude Control

Inertial Attitude Reference - This software sizing was slightly redesigned to add attitude error compensation and to change some data to single precision.

Table 3-3. SEPS Planetary Mission Software Sizing Summary

	INSTRUCTIONS (16-BITS)	DATA (16-BITS)	TOTAL (16-BITS)	SPEED (KAPS)
EXECUTIVE	1115	1060	2175	0.72
PROPULSION	1203	273	1476	0.92
ATTITUDE CONTROL	1813	670	2483	0.81
GUIDANCE AND NAVIGATION	30	80	110	0.03
DATA HANDLING*	140	602	742	0.14
COMMUNICATIONS	1519	415	1934	0.47
SOLAR ARRAY	150	30	180	0.15
POWER DIST.	150	200	350	0.15
MECHANISMS	0	105	105	0
THERMAL	0	0	0	0
REDUNDANCY MANAGEMENT	1242	355	1597	1.19
SCIENCE PAYLOAD	150	50	200	0.01
TOTAL			11352	4.59

*Does not include 4K telemetry data requirements.

Table 3-4. SEPS Earth Orbital Mission Software Sizing Summary

	INSTRUCTIONS (16-BITS)	DATA (16-BITS)	TOTAL (16-BITS)	SPEED (KAPS)
EXECUTIVE	1115	1060	2175	0.72
PROPULSION	1203	273	1476	0.92
ATTITUDE CONTROL	1853	835	2688	0.85
GUIDANCE AND NAVIGATION	1820 (9330)	277 (1767)	2097 (11097)	1.14 (2.50)
DATA HANDLING*	140	625	765	0.14
COMMUNICATIONS	1064	322	1386	0.24
SOLAR ARRAY	150	30	180	0.15
POWER DIST.	150	200	350	0.15
MECHANISMS	0	125	125	0
THERMAL	0	0	0	0
REDUNDANCY MANAGEMENT	1342 (1642)	405 (555)	1747 (2197)	1.29 (1.59)
TOTAL			12989 (22439)	5.60 (7.26)

( ) - High-autonomy G&N (optional)
*Does not include 4K telemetry data requirements.

Star Tracker Processing - The previous SEPS study had baselined the use of star mappers rather than star trackers. This sizing reflects a substantial reduction in storage requirements which resulted with the change to star trackers. The difference in the amount of data required for planetary and earth orbital missions is due to the larger star table required for the earth orbital missions.

TVC/RCS Processing - This module sizing increased slightly due to the current TVC design having all engines gimballed rather than having only four engines gimballed for roll control and pitch and yaw control performed by X-Y translators. The larger sizing for earth orbital missions reflects the requirement for RCS translation control for docking.

For more detail on the attitude control subtask descriptions, see Page 6-16 of Reference 2 and Page A-18 of Reference 1.

3.2.2.4 Guidance and Navigation

Planetary Missions

No change is recommended for this sizing. See Page 6-17 of Reference 2 for further details.

Earth Orbital Missions

This sizing was changed significantly from the last study to refine and incorporate functions which had previously been identified as optional. Two cases were sized:

1) Low Autonomy case where significant ground interface is involved, with communications taking place once each day.

2) High Autonomy case where minimum ground contact is involved, with a near optimal guidance scheme programmed onboard.

The baseline selection is the low autonomy case which is consistent with current Rockwell International studies. However, the high autonomy concept is being retained as an optional configuration. Reference 12 documents a study by IBM concerning low vs. high autonomy SEPS.

Detailed software G&N subtask descriptions for the baseline SEPS concept follows:

Mid-course Guidance

A polynomial guidance scheme was selected for the baseline sizing. This scheme generates polynomials of guidance commands based on an independent variable which is chosen to yield the simplest polynomial. The two-axis guidance commands are used as inputs to the attitude control routines.

State Propagation

This software module integrates the equations of motion to determine SEPS velocity and position. These parameters are used to determine the local vertical reference frame and the argument of latitude. Parameters may be updated from the ground.

Sun Direction Determination

This routine computes the sun vector and transforms the data to the computational coordinate system to generate attitude control commands. Normally, sun sensor output data is used by this routine, but it is capable of determining the location without sun sensor input.

Navigation Update

For the baseline, low-autonomy concept navigation updates are not calculated onboard but are transmitted to the SEPS by ground command.

Target State Propagation

This routine integrates the equation of motion of the target to determine target position and velocity. These peremeters can be updated from the ground.

Laser Radar Processing

This routine smooths and biases the laser radar data to improve the data accuracy for rendezvous.

Rendezvous Guidance

This routine uses the vehicle state vector, the target state vector, and laser radar information to determine the relative position and closing rates of the SEPS with the target and to compute the guidance commands required for rendezvous.

Mode Control

The mode control commands are associated with the phases of the mission, such as mid-course, coast, rendezvous, and docking. The mode commands are set to initiate the required functions during the different mission phases.

3.2.2.5 Data Handling

This function has been incorporated into the CCS. Two subtasks were sized:

Telemetry Processing

This software sizing was increased due to an increase in the number of parameters to be telemetered from 336 to 578 for planetary missions and 601 for earth orbital missions. See Page 6-17 of Reference 2 for additional details.

Data Storage Management

This item replaces and expands upon the "Tape Recorder Control" sizing contained in Rockwell International study Exhibit E. In addition to tape recorder control, there is the requirement to control the buffer storage. Additional logic is sized to control the transfer of data between buffer storage (in main memory) and the recorder, and between these components and the communications subsystem.

3.2.2.6 Communications

Planetary Missions

Antenna Pointing and Control - This sizing was increased slightly to account for the logic required to switch low gain antennas automatically. See Page A-27 of Reference 1 for additional detail.

Command Processing - This sizing is based upon processing 324 ground commands with 55 requiring special command processing. This includes 64 and 14, respectively, for science payload commands. See Page A-27 of Reference 1 for additional details.

Mode Control - See Page A-27 of Reference 1 for details.

Earth Orbital Missions

Low Gain Antenna Switch - This software was added to account for the logic required to switch low gain antennas automatically.

Command Processing - This sizing is based upon processing 259 ground commands with 39 requiring special command processing. See Page A-27 of Reference 1 for additional details.

Mode Control - See Page A-27 of Reference 1 for details.

3.2.2.7 Solar Array

Solar Array Length Control - This sizing has been reduced to reflect that the solar array length control is commanded from the ground and no automatic

control is provided on board (i.e. automatic solar flare detection). Some logic is still required to respond to the ground commands.

Peak Power Computation

This software was added to more accurately determine peak power available from the solar arrays. A power curve will be stored in the onboard computer and periodically updated by monitoring the real available power from the solar arrays. This data will be used by the propulsion subsystem for power level and power margin management.

3.2.2.8 Power Distribution

In previous studies, the only power distribution software that was considered was associated with redundancy management (i.e. no power distribution control software was sized). For this study, however, the onboard computer will perform the logic necessary to perform functions such as power calculations, battery charging control, orderly power down of equipment to the keep-alive mode, initial equipment power-up sequencing, and measurement feedback monitoring. Since detailed operating modes and computer functional requirements for power distribution have not been defined, this software sizing estimate is considered preliminary, and emphasis should be placed on refining this sizing during follow-on studies.

3.2.2.9 Mechanisms

Planetary Missions

The only change to this software was a reduction in the Antenna Deployment sizing to reflect that the omni antennas do not require deployment. See Page A-31 of Reference 1 for additional data.

Earth Orbital Missions

The only change to this software was the deletion of the function Antenna Deployment because the omni antennas no longer require deployment. See Page 3-10 of Reference 1 for additional data.

3.2.2.10 Thermal

There is no software logic required for the thermal subsystem. All heaters are thermostatically controlled with ground override command capability.

3.2.2.11 Redundancy Management

Planetary Missions

CCS/DHS

The sizing for the computer and data handling was combined into one sizing. The computer sizing was left unchanged. The only data handling functions which were sized were temperature and servo phase detector monitoring of the tape recorders to detect failures so that the redundant tape recorder could be used.

Power Distribution

This sizing combined the sizing for Electrical Power and Stage Power and Distribution functions.

Communications

This software was added in this study to perform redundancy management on the following components: S-Band TWTA, X-Band TWTA, S-Band Exciter and Receiver.

See Page A-31 of Reference 1 for additional details.

Earth Orbital Missions

Deltas are the same as planetary missions with the following exceptions.

Guidance/Navigation

Added additional sizing for the autonomous G&N case to account for more detailed redundancy management that is required.

Communications

This software was added in this study to perform redundancy management on the following components: TV Telemetry Section (TTS) Transmitter, TTS Exciter, S-Band Exciter and Receiver.

3.2.2.12 Science Payload

This software module was added during this study to reflect onboard computer requirements for a typical science package for a planetary mission. It specifically includes a Scan Platform and Magnetometer Bias control. Also, a small amount of additional software was included to provide simple sequencing functions in response to a ground command to initiate the science sensors.

CCS FUNCTIONAL DESIGN 4

4.1 GENERAL

This section describes the definition of the baseline CCS design. Recent changes have occurred in the SEPS program which had to be evaluated to determine their CCS design implications. These changes were:

- Updated software sizing requirements (Reference Section 3.2)
- Updated CCS interface definition (Reference Section 3.1)
- 1976 technology cutoff date
- New CCS reliability allocations (Reference Section 5)
- Addition of dual redundant tape recorders to the CCS
- Requirement for the CCS to temporarily store up to 4K of 16-bit telemetry words (Reference 4.2.4 below)
- Incorporation of the bulk of the SEPS subsystem data acquisition functions into the CCS (Reference 4.2.3.2.1 below).

Various computer configurations were considered to determine the most cost effective design which could meet the SEPS requirements. The CCS reliability requirement of 0.95 for a three-year, unmaintained mission was the requirement which was the configuration driver. To meet this stringent requirement, the fault tolerant memory configuration was chosen based on cost, weight and volume considerations. (Reference Section 5 for the Reliability and Redundancy Management Analysis). And, in particular, the fault tolerant version of the HTC was chosen to comprise the basic element of the CCS.

4.2 DESIGN CONSIDERATIONS AND DESCRIPTION

4.2.1 TECHNOLOGY SELECTION

The previous study (Reference 2) carried two technology baselines, one a 1973 TTL baseline and the second a 1975 CMOS baseline. The current study groundrule is a 1976 technology, and IBM has selected this to be TTL for the following reasons. First, custom low-volume/low-cost CMOS chips are not currently available nor projected to be available by the 1976 time period because of vendor policies which directly impact customization. Principle CMOS vendors are tending to offer low prices for very high production devices and to discourage custom chip designs with higher prices, because small quantity buys of customized CMOS produces low and unpredictable yields. Second, the failure rate data for LSI CMOS devices is not as reliable due to their relative newness as compared with the long term, wide data base developed for TTL devices derived through extensive military, NASA, and commercial usage. Third, low cost custom TTL or bi-polor LSI is available with integration levels greater than 130 gates per chip from high volume commercial users. Finally, MSFC support of the SUMC in the highly reliable and fault tolerant areas is being developed in TTL logic. Examples are the design of system logic chips for the translator and the demonstration of a design of a TTL compatible fault tolerant memory.

Bi-polor technology selection does not preclude the use of other technologies required for special applications. An example is the use of N-MOS Basic

Storage Modules (BSM's) that uniquely satisfy the single bit-per-BSM requirement as defined in the previous SEPS study report (Reference 2) for the fault tolerant memory.

4.2.2 COMPUTER DESIGN

After reevaluation of the computer considering the revised requirements, no significant changes were found to be necessary to the basic computer configuration as proposed in the previous study. A five fault tolerant memory, redundant CPU's, error correction translators, power supplies, switching circuits, and support hardware were found to be required to meet the CCS reliability goal. During this study period the Hybrid Technology Computer (HTC), a member of the SUMC family of computers, was delivered to MSFC. Its increased programming flexibility derived from the Systems/360 instruction set and its functional slice packaging technique (a CPU/slice) are representative of the concepts necessary for the implementation of the functionally redundant low cost SEPS computer.

4.2.2.1 Main Memory

The fundamental approach of the five fault tolerant main memory has not changed from that presented in the previous study except that the maximum memory size estimate has increased to approximately 13K of sixteen-bit words.

To maintain adequate contingencies, 20K words of storage are necessary to provide about 50% spare memory capacity without incorporation of a 4K telemetry memory buffer (Reference Section 4.2.4 for a trade study concerning incorporation of the telemetry buffer into the main storage). For 8K x 1 bit

of storage in the fault tolerant configuration, twenty-six of the Basic Storage Modules (BSM) are required (16 for data, 6 for check bits, and 4 spares). Some separate memory support logic is also necessary. For 20K of storage, 78 BSM's are required: 52 BSM's containing one 8K x 1 bit chips and 26 containing one 4K x 1 bit chips. The depopulation of 26 BSM's helps to conserve power. To minimize non-recurring costs, full addressing capability is retained for a potential memory increase to 24K x 16 bit words. Full population of three 8K pages would require 78 BSM's containing one 8K x 1 bit chips.

4.2.2.2 Translator/CPU

Translator

Design of the translator has produced three significant improvements. Two involve the input/output reconfiguration switches.

First, the BSM input reconfiguration switches have been eliminated. When a failed BSM is detected, a spare BSM is assigned the same bit position as the failed BSM. Both receive data after correction is achieved by the translator in an automatic read-correct-write cycle. The output of the failed BSM is then disconnected, but its input remains connected. Only one BSM reassignment is made at a time as opposed to adding a BSM at the end of a word and "bumping" the contents of each BSM down one position. This was equivalent to a shifting operation and involved more BSM switching hardware than individual replacement. In addition, the new technique should be faster.

The second change in the concept reflects that it is more efficient to design translators in conjunction with the CPU and to dedicate a translator to a CPU rather than switching a translator between CPU's. This precludes uneven distributions of translator and CPU's and eliminates switching complexity between CPU/translator.

The third design improvement was its implementation in self-testing (similar to two rail) logic which is dynamically self-checking and allows immediate indication of a translator error. Spare translator/CPU's can then be switched into the system upon error detection.

CPU

Four SUMC CPU options with an 8K x 16-bit non-fault tolerant memory were considered for CPU trades, and trade data are presented in Table 4-1. The previous baseline was the 8-bit SUMC CPU executing 47 aerospace instructions. As seen from this table, the 16-bit data flow TTL-LSI CPU has an advantage in programming ease using the S/360 86 instruction set because it is a familiar set easily programmed with extensive software tools available to the programmer. Its average power is not significantly higher than the others, and in a triplex configuration the failure rate results in an acceptable reliability for three years (Reference Section 5 for reliability details). Its weight is comparable with all other CPU candidates except the N-MOS LSI, but that technology has a high development cost and risk. All units have adequate throughput capability. The higher the speed provided, the lower the average

Table 4-1. SUMC CPU Trade Data

DATA FLOW	TECHNOLOGY	INSTRUCTION SET	SYSTEM POWER PEAK/AVG (WATTS)	CPU FAILURE RATE $X10^{-6}$	SYSTEM WT (Kg)	SPEED (KOPS)	RELATIVE DEVELOPMENT RISK	SYSTEM NON-RECURRING COSTS (RELATIVE)	SYSTEM RECURRING COSTS (RELATIVE)
8-BIT	TTL LSI	4π(TC 2),47	45/10	2.82	3.6	150	2	1.1	0.9
8-BIT	TTL LSI	S/360, 80	54/11	4.42	3.6	65	2	1.1	0.9
8-BIT	N-MOS LSI	S/360, 80	25/8	2.59	1.4	100	10	1.4	0.8
16-BIT (HTC)	TTL LSI	S/360, 86	60/13	5.56	4.6	250	1	1	1

o Previous Baseline - 1973 Technology

oo Recommended Current Baseline

power required since a low duty cycle is possible and power switching can effectively reduce the average power consumed. The 16-bit HTC has the largest speed capability of these options and, hence, the most potential for power savings by selective power switching. Finally, the development and production costs of the 16-bit data flow HTC are significantly lower because it is a developed product which will be partially qualified for space environments in time for the SEPS missions (MIL-E-5400 Class 2X).

4.2.2.3 Clock

Continuous clock signals must be supplied to the memory and translators. Accordingly, the previous study proposed a design for fault tolerant clock and logic timing circuits. TMR plus one spare redundancy was proposed in the previous study (See Figure 4.1.3 of Reference 2), and this redundancy has been retained in this study.

The previous study recommended that the dual redundant power supplies be operating at all times which allowed for powering the TMR plus spare clocks. In this study phase it was found more advantageous from power and weight considerations to operate only the TMR oscillators and clock circuits until switchover to a redundant power supply can be achieved, nominally within 10 msec. Since power must be retained on the monolithic N-MOS memory at all times, it is recommended that small, battery power supplies be included in the CCS to power clocks, reconfiguration switches and main memory in the event of bus or regulated power supply failure. Normally, the batteries would be floating slightly under normal bus levels but kept charged by the power distribution subsystem at a trickle charge rate.

4.2.2.4 Reconfiguration Control

The reconfiguration control concept for the CCS has not changed from the previous study (See Reference 2, Figure 4.1.6) except that a more definitive technique for attaining high coverage has been designed for the CPU, translator and power supply. For the CPU a coded self-test is currently being evaluated under contract to MSFC which will detect CPU faults. The previously defined CPU window timers are retained; however, the CPU self-test is now predominately macro-oriented rather than microcoded. It requires approximately 150 machine instructions and an execution time of about 1.6 milliseconds with the baseline CPU executing a System/360 fixed point instruction set. Since the CPU speed is high and SEPS computation time requirements are low, the self-test may be run many times per second making it highly effective. Note that no additional microprogrammed Control Store or microcontrol read-only-memory (MROM) is required for this approach, which uses three elements for CPU fault detection:

(a) Special macro tests

(b) Hardwired window GO/NO-GO timers

(c) Use of existing machine check and program check interrupts to stop the GO/NO-GO timer

4.2.2.5 Power Supply

A three power supply configuration has been retained; however, they are now implemented in the highly reliable hybrid design currently used in the HTC. A minimum of 10 milliseconds power switchover time to an essentially no-load or standby supply has been demonstrated. The minimal current to be drawn by

the supply and its recovery time to within specification limits requires further study for this particular application. No-load on supplies tends to cause instability and to slow power-up events, while partial load (<20%) dissipates useless power and contributes to unreliability. Acceptable switchover times need to be established for CCS detection, reconfiguration, and restart.

To conserve power the CPU, translators and main memory are placed in a low power mode when not being actively used. This is particularly beneficial for SEPS applications because of its low duty-cycle requirement. ON/OFF demand power switching is used for the CPU and translators and the utilization of a low power mode is used for the memory. Memory voltages are lowered when an 8K x 16-bit module is not enabled. Lowering supply voltages retains memory content while reducing consumed power. Reconfiguration switches and TMR clocks are powered at all times. The active tape recorder is powered only during infrequent write/dump modes. Only one customized I/O is powered at a time. However, certain portions must remain powered in the operating I/O. This topic is discussed more fully in Section 4.2.3.

Table 4-2 presents average CCS power requirements including power supply inefficiency of 65%.

4.2.3 CUSTOM I/O DESIGN

One of the major tasks of this study was to review, reassess and revise the preliminary design of the custom I/O documented in Reference 2. Emphasis

Table 4-2. Average CCS Power Requirements

	20K MEMORY + 4K TM BUFFER	24K MEMORY (NO TM BUFFER)
COMPUTER*	24.4	28.1
CUSTOM I/O**	12.3	12.3
TAPE RECORDER	2.0	2.0
4K BUFFER	4.6	-----
	43.3 WATTS	42.4 WATTS

* INCLUDES 16-BIT CPU & ALL BSMs POWERED

** DOES NOT INCLUDE CIRCUITS EXTERNAL TO CUSTOM I/O

was placed upon defining I/O hardware to interface the CCS with other SEPS subsystems.

4.2.3.1 General Description

The custom I/O provides the capability of interfacing the general purpose SUMC computer with the SEPS subsystems. It is composed of two identical halfs, but only one-half of the I/O is powered-on at any given time. To further conserve power, power switching techniques are applied inside the I/O. The custom I/O contains a redundant command subsystem interface for accepting ground commands. All custom I/O operations, with the exception of the command subsystem, are controlled by the CPU. Data flow to and from each I/O section is via two sixteen-bit buses, which interface with three CPUs via the switching logic. A block diagram of the custom I/O interfaces with the CPUs and the other SEPS subsystems is shown in Figure 4-1.

A hybrid I/O approach was baselined for the SEPS program. This means that the I/O physical package contains most of the required receiver and driver circuits necessary to interface directly with each subsystem. Direct interface is achieved with all SEPS subsystems, except the solar array and the propulsion subsystems. Serial data transmission is used to interface with these two subsystems. This centralized approach to data acquisition is the major difference between the current design and the design documented in Reference 2.

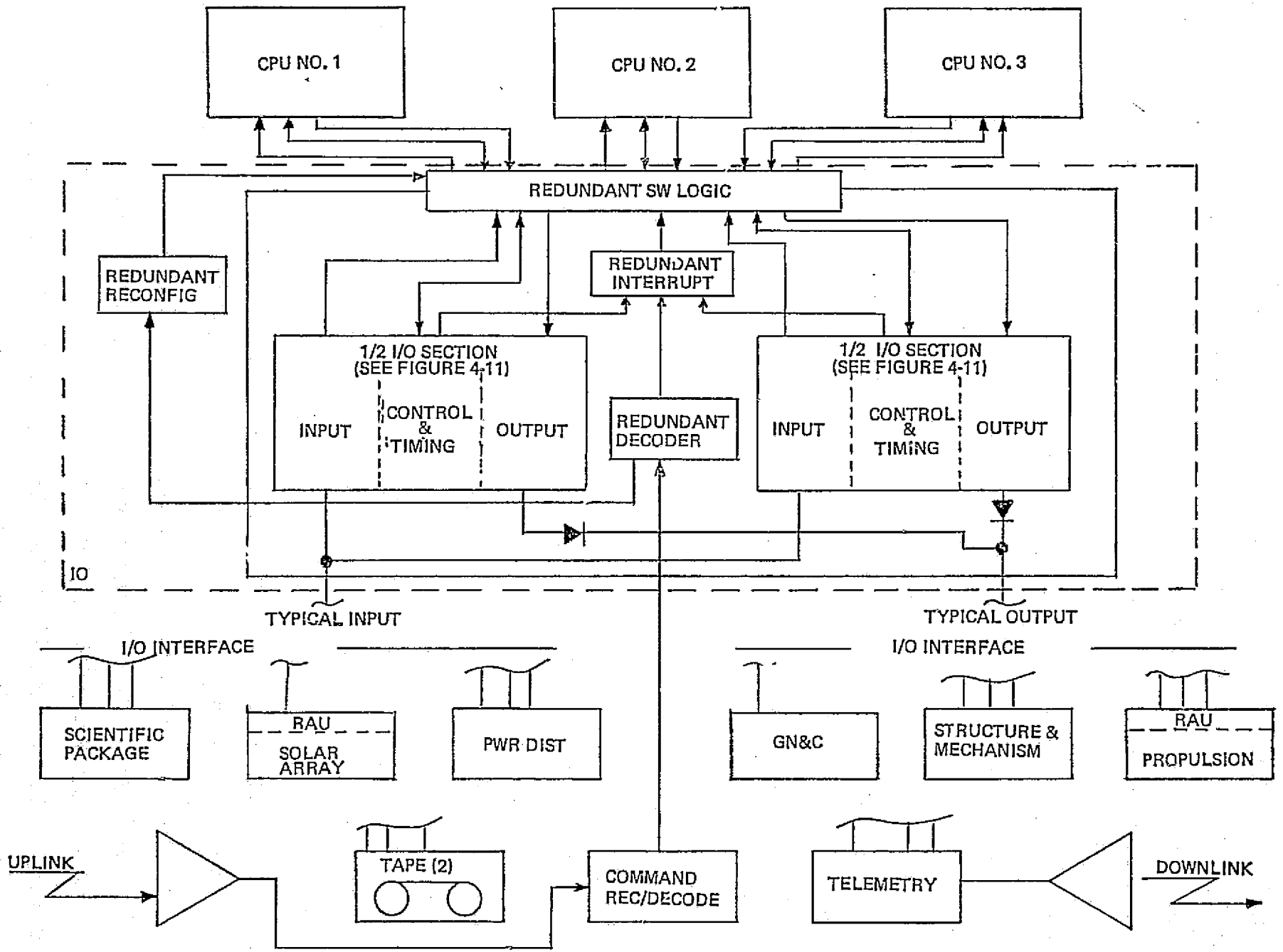


Figure 4-1. Custom I/O Interfaces

Each half I/O section contains an input section, an output section and a timing and control section. The input section contains receivers, converters, registers and gates necessary to control the input signal onto the 16-bit data bus. The output section contains registers, gates and drivers to generate the required outputs to the various SEPS subsystems. The timing and control section interfaces with the CPU switching logic and directs bus traffic.

Output signals from each half I/O section, which are driving a simplex subsystem, are diode isolated and connected together inside of the I/O. Simplex inputs to the I/O are internally connected to both half sections.

The command interface logic of the I/O is Triple Modular Redundant (TMR). Three identical sections contain receiver circuits, 16-bit input registers and decode/control logic. The register outputs are connected to the I/O input bus through voter isolation circuits. Interrupt flags from the command interface logic advise the CPU when data is being received and/or when the command register is full. Special commands can be received which bypass the normal CPU input path.

The custom I/O will direct and control data to and from the telemetry buffer whether the buffer is located in the fault tolerant main storage (baseline) or as an external unit. Telemetry formatting is performed by software. Data fetch commands are generated by the CPU and responses from the subsystems are loaded directly into the telemetry buffer. Discrete outputs for controlling the tape recorder and buffer (if external) are channeled directly to discrete output registers in each I/O section.

The following sections describe trade studies which were performed and give details of the I/O design.

4.2.3.2 I/O Design Trades

Two major design trades were conducted during this study. One was centralized vs remote data acquisition, and the other was an interface circuitry concept trade. These analyses are described below.

4.2.3.2.1 Remote Versus Centralized Data Acquisition

A study was performed to determine the relative merits of a centralized acquisition unit vs a set of remote data acquisition units for data collection, conditioning and control. This section describes the advantages of each approach and recommends a baseline design.

Remote Data Acquisition

A system utilizing remote acquisition units which converts, formats and codes/decodes data remotely from the CCS and communicates that data to and/or from a centralized interface device via a single channel is shown in Figure 4-2A. This system would utilize a standard-design remote unit placed as required at the major subsystems. The advantages of a remote acquisition system are discussed below:

a. EMI characteristics - Conversion of analog signals would take place in close proximity to the subsystem where the analog measurements were being taken. The transfer of data to/from the centralized unit would be in the form of a digital word; therefore, certain error checking (at least parity) could be easily accomplished.

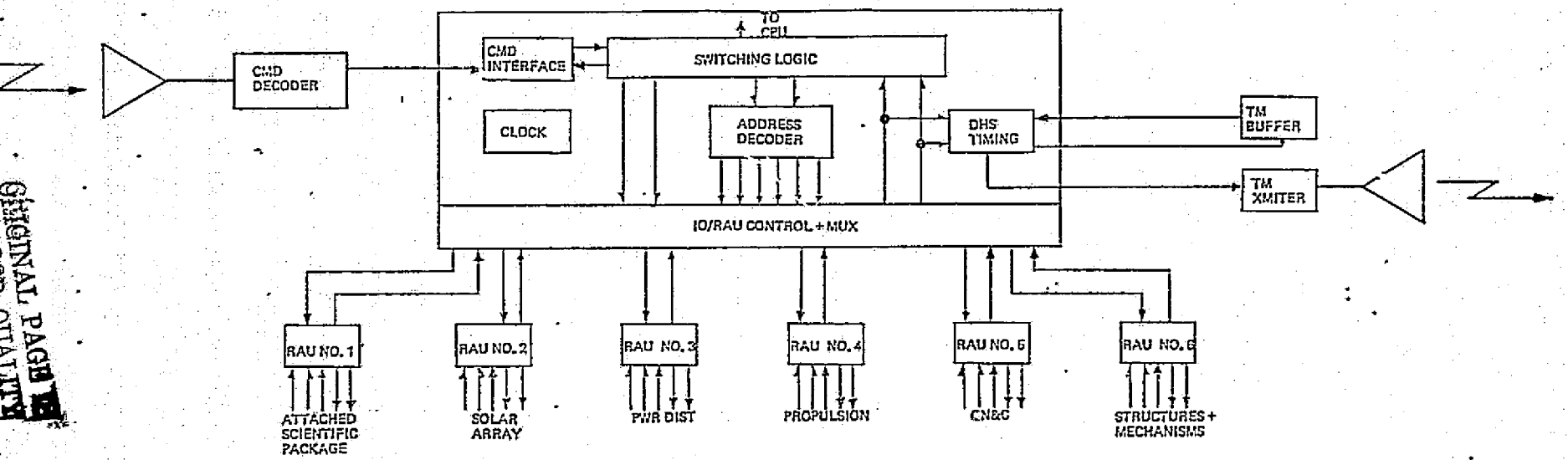


Figure 4-2A. Distributed I/O Approach

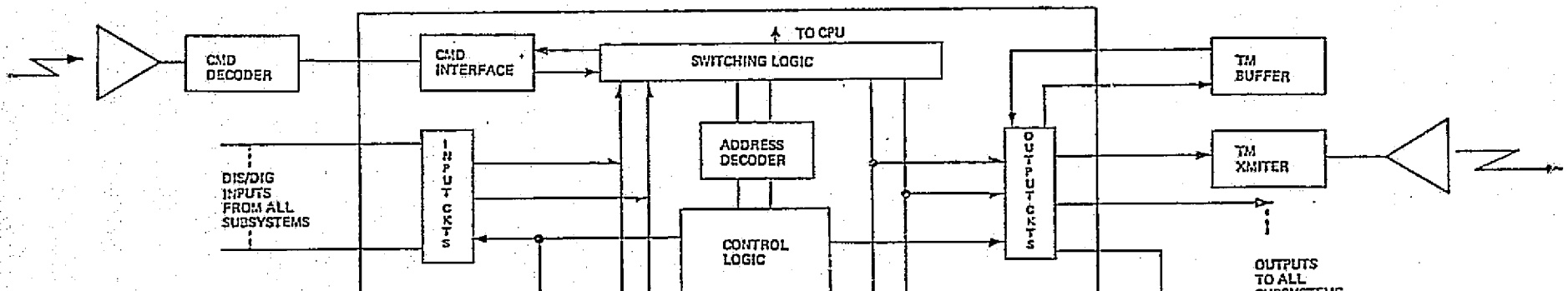


Figure 4-2B. Centralized I/O Approach

b. Maintainability - Maintainability prior to launch would be enhanced by the use of six RAUs as opposed to one centralized I/O. Logistic spares for the smaller RAUs could be easily handled, tested, and stored.

c. Physical mounting - Mounting of a set of RAUs would be more expedient, due to the fact that a small isolated space near the subsystem could be used to mount an RAU. A centralized I/O would require a larger area for mounting.

d. Heat dissipation - Heat dissipation on a distributed system is more even. This results in few, if any, "hot spots" and better heat transfer qualities for the equipment bay.

Centralized Data Acquisition

A centralized I/O is one in which all multiplexing, conversion, coding and formatting is done at a centralized location, usually a single structure, and the interface with the CPU is made via a single data path. A block diagram of a typical centralized I/O is shown in Figure 4-2B. Advantages of a centralized I/O are listed below:

a. Spacecraft size - The small size of the SEPS equipment bay lends itself to a centralized approach with the longest cable run less than ten feet.

b. Equipment size and weight - The centralized approach would save weight and volume. Fewer partitioning walls, structures and connectors would be required. Volumetric efficiency would be enhanced by more efficient usage of input/output circuitry, i.e., a standard

I/O for an RAU might have only 40-50 percent usage at one location and another subsystem would be overloaded with few or no spare I/O circuits. In a centralized approach, the input/output circuit can be distributed evenly among various subsystems.

c. Power distribution - Power distribution to the I/O circuitry is greatly enhanced by the centralized approach. With all I/O circuitry located in one structure, power distribution is internal to the I/O box, thus minimizing noise and IR losses in the power lines. In a remote acquisition system redundant power would be distributed to each remote acquisition unit. This would increase power supply regulation problems, noise problems on power lines and cable weight.

d. Reliability - In a single structure, reliability is enhanced since switching control lines are self-contained and are not cabled external to a centralized I/O box. This saves weight, reduces the possibility of noise injection on switching lines, and increases reliability.

Conclusions

Table 4-3 gives a summary of the centralized vs remote data acquisition analysis. Primarily because of advantages in weight, power and reliability, a centralized approach is recommended. However, there are two SEPS subsystems which should be treated as special cases. These are the solar array and propulsion subsystems.

Table 4-3. Centralized vs Remote Data Acquisition Trade

Parameter	Centralized I/O	Distributed I/O
EMI Compatibility	+	
Weight/Size	+	
Heat Dissipation		+
Power Distribution	++	
Reliability	+	
Packaging		+
Maintainability		+
Spacecraft Mounting		+
Spacecraft Cabling	+	

Legend: + = Slightly Better

++ = Significantly Better

Solar array subsystem - There are approximately 250 temperature, voltage and current measurements originating in the solar array subsystem. Because of the volume of measurements to be handled, it is recommended that a combination multiplexer/analog-digital converter be located at each solar array wing to reduce the number of input signals to the CCS.

Propulsion subsystem - The power processor units in the propulsion subsystem contain analog/digital converters, conditioners and formatters which accomplish the function of data acquisition. Therefore, the only accommodations required of the I/O is to interface with serial digital lines from the propulsion subsystem.

4.2.3.2.2 Interface Circuit Concepts

SEPS CCS interface concepts must be defined prior to detailed hardware specification. Three important inter-related factors must be considered in selecting interface circuit concepts. They are:

1. Electromagnetic interference compatibility
2. Failure independence related to redundant interfaces
3. Failure detection philosophy associated with redundancy management

High electromagnetic interference levels are anticipated on SEPS because of the noise-generating nature of the solar electric engines. Although specific levels have not been determined, interference signals could easily be greater than the three volts expected as a result of Viking experience (Reference 3). Techniques are available to permit reliable operation in a noisy environment without risk. However, these techniques are more complex than those used on

Viking. In addition, CCS reliability requirements dictate I/O redundancy. This consideration is also instrumental in defining interface concepts.

Related to interface definition is failure detection and redundancy management. Redundancy management can influence both I/O circuit design and the quantity of circuits involved.

This section treats each of these aspects independently and then recommends concepts which take combined aspects into account.

EMI Interface Interconnection

Methods of minimizing EMI effects are well understood. Principles can be applied to inter-unit communication to reduce unnecessary interference and permit proper operation in a relatively noisy environment. Since the CCS signal interface consists of several hundred measurements and commands, overdesign could result in excessive reliability, power, weight and cost penalties. Thus, tradeoffs are in order.

The approach recommended is to employ conservative engineering practice when penalties are not severe and design so that noise rejection levels are predictable and can be improved by additional shielding. Clarification of this point is the subject of the following discussion.

Fundamentals of EMI compatibility are well documented (References 4 to 7). Interference is unwanted signal noise coupled directly by power distribution circuits or indirectly by radiation and conduction (common impedance current

paths). Noise injection directly through the power system is controlled by unit power supply requirements and is not discussed here. Of interest is the interference introduced via signal interface wiring. Fundamentals are reviewed briefly prior to evaluating interconnection options.

EMI Compatibility

Interference coupling is accomplished by electric field (capacitive coupling), magnetic field (inductive coupling), and common impendance conduction. The most troublesome radiation coupling is via strong, low-impedance magnetic fields. Key parameters for reducing magnetic field coupling are shown in Lenz's Law:

$$V = -nA\frac{d}{dt}B$$

where,

V = open circuit induced voltage

n = number of turns

A = circuit area

B = magnitude of the field

$\frac{d}{dt}$ = time rate of change (frequency)

Thus, inductively coupled interference voltage can be reduced by decreasing the interference field strength, B, the circuit area, A, and the interference frequency.

Shielding is generally effective in reducing electric field energy, independent of frequency, and magnetically coupled energy at high frequency. Conversely stated, shielding has minimal effect in attenuating strong magnetic

fields, especially at low frequency, so that reducing the area of the interface circuit is important.

Figures 4-3 and 4-4 taken from Reference 5 illustrate this point. Sixteen circuit configurations are shown (Figure 4-3) along with the induced voltages (Figure 4-4). The greatest difference in pickup occurs between circuit #5 and circuit #6. Circuits #1 to #5 provide an alternate return path through the ground plane, thus increasing the area of interference exposure. Shielding has little effect at the low 400 Hz interference test frequency. When the ground plane return path is not provided, twisting the signal wires reduces circuit area (and provides some cancellation) and further minimizes interference pickup.

Loveland and Goodwin (Reference 8) tested several cable types and also compared EMI susceptability to an unshielded reference wire. Their work (see Figure 4-5) also illustrates the aforementioned principles but, in addition, shows the cable/shielding effectiveness as a function of frequency. Circuit configurations for their tests were similar to circuit #4 for the coax sample and circuit #9 for the twisted shielded pair. Note that significant interference attenuation over a wide frequency range is demonstrated via balanced transmission and twisted shielded cabling. Shielding accounts for high frequency noise rejection and twisting, and balanced reception provides low frequency rejection. Balanced reception is implemented via transformers, relays and differential amplifiers.

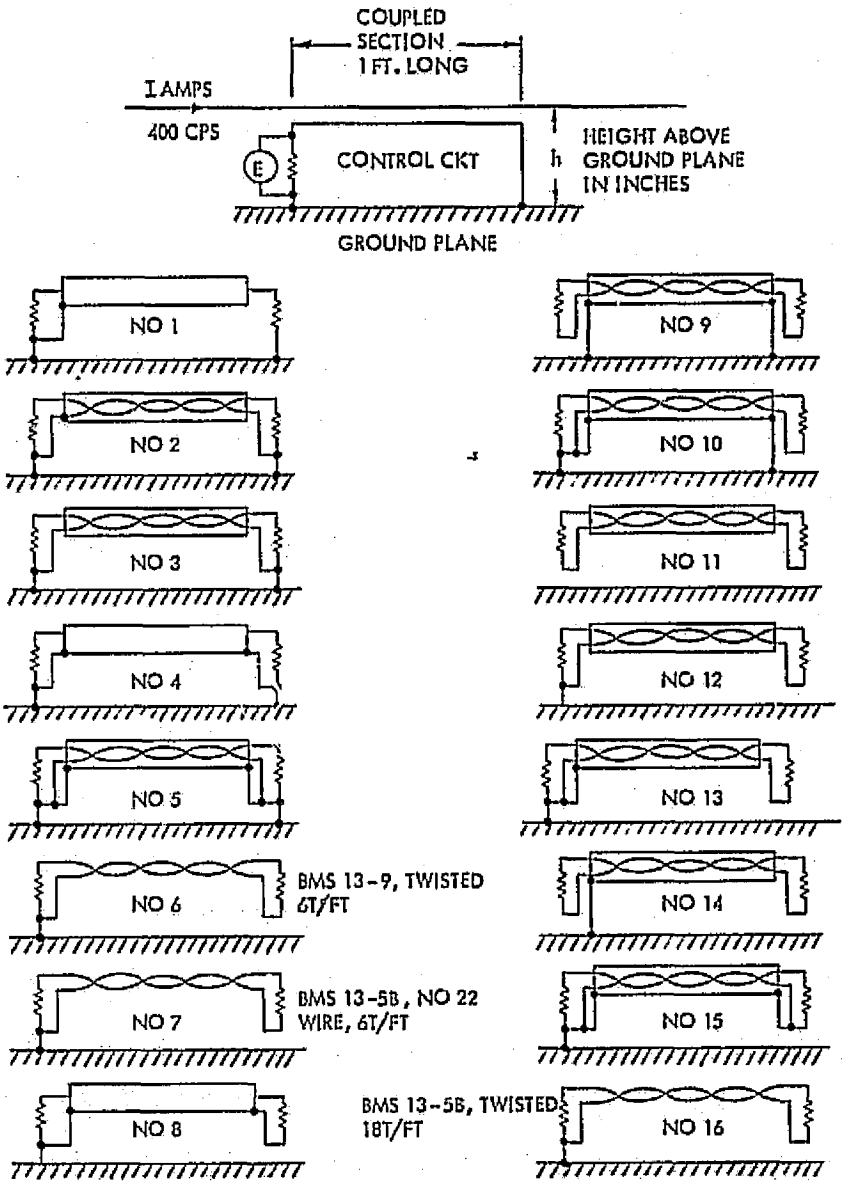


Figure 4-3. Cable and Shield Configurations

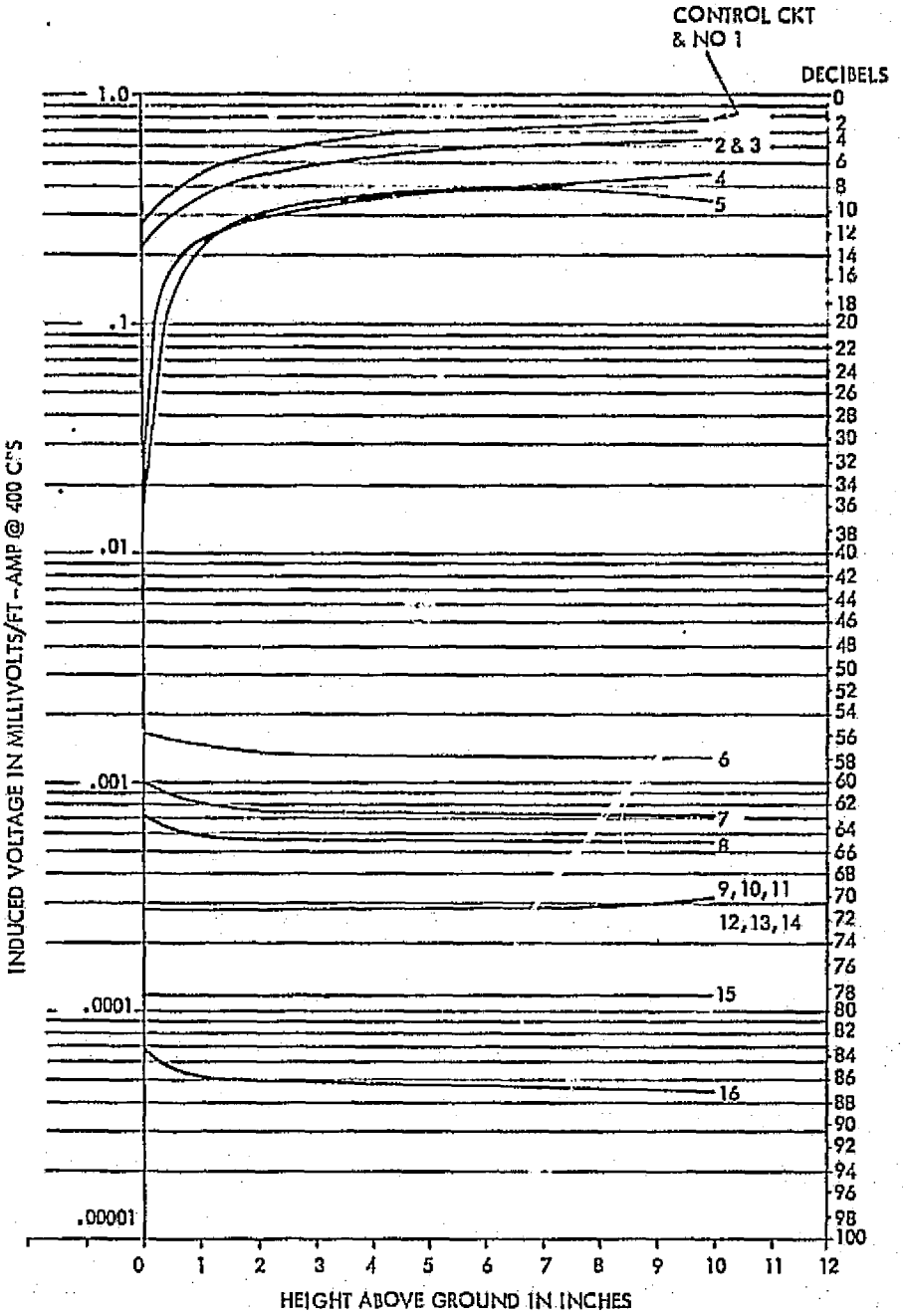


Figure 4-4. Induced Voltage Using Figure 4-3 Configurations

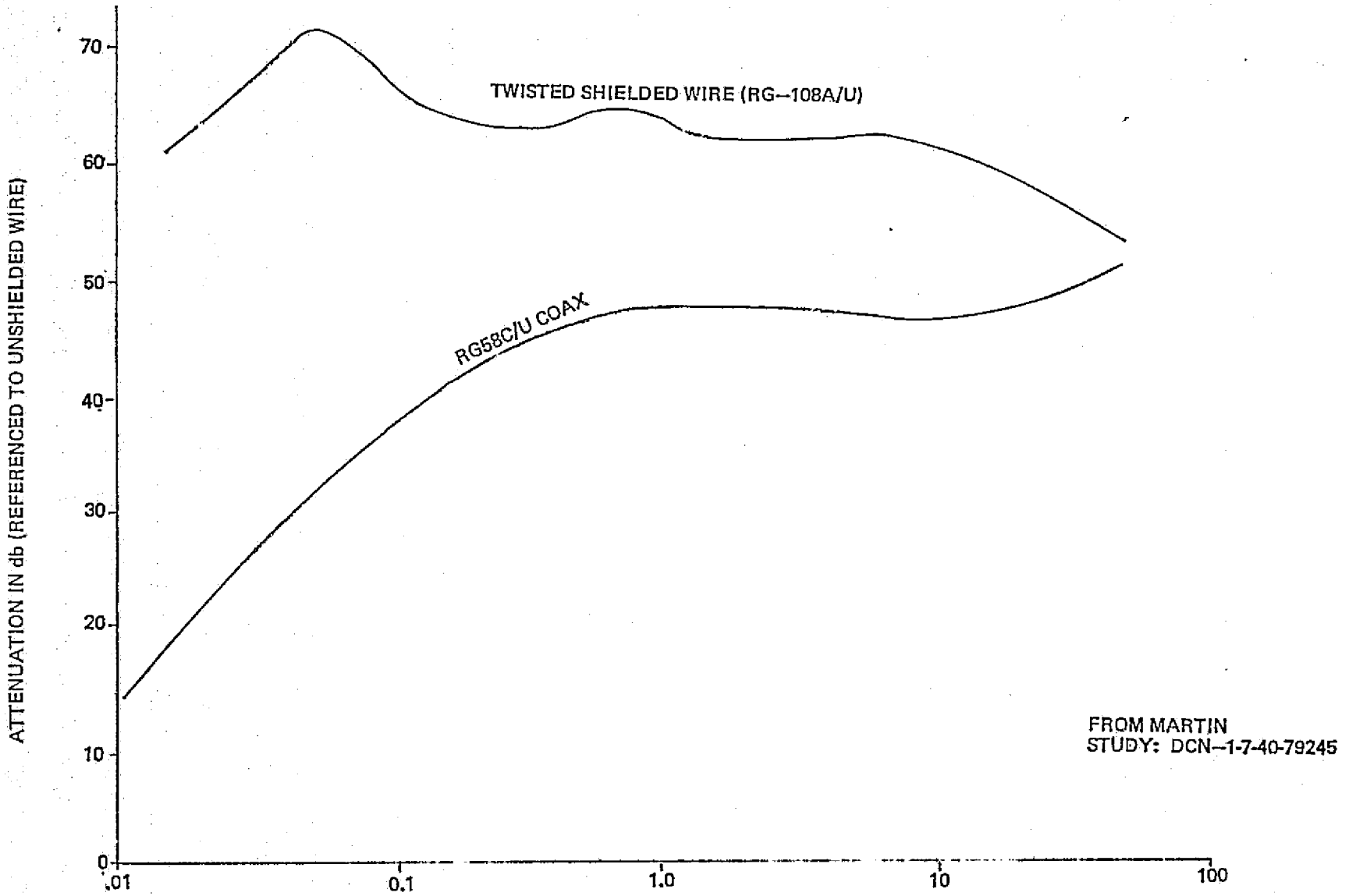


Figure 4-5. Noise Attenuation of Typical Cable

Mohr (References 9 and 10) formulated expressions for predicting interference coupling levels in various cable types above a ground plane. His analysis includes noise sources of both a sinusoidal and transient nature. Figure 4-6 is a graph from Reference 10 showing coupling from a transient source into (1) an unshielded specimen, and (2) a shielded RG58C/U coax. Parameters were selected as representative of a typical SEPS cable configuration.

For a quantitative example applicable to SEPS, consider two parallel five-foot cables, impedances as given in Figure 4-6, and a 10 ampere current transient of one microsecond rise time. Coupling into an unshielded cable will produce a peak interference signal V_c = 0.19 times 10 amps times five feet = 9.5 volts. Into the shielded line V_c = (0.0014) (10)(5) = 0.07 volts. Thus, shielding can be extremely effective if interference coupling can be restricted to higher frequencies via radiated paths. The amount of coupled interference is a direct function of frequency, but fortunately the magnitude of low frequency noise is also lower. Curve one, of Figure 4-7, illustrates noise induced into an RG58C/U sample as a function of frequency. As indicated, shield effectivity begins at about 1 KHz. Curve two shows the typical effect of double shielding. This curve was generated by squaring the shield attenuation factor provided by RG58C/U and is shown for illustration only. It does suggest that high frequency noise can be substantially eliminated by properly applied shielding, and that noise from one to 10 KHz will be most troublesome.

In the previous discussion, all coupling is from a single interference cable source into a single test specimen. The analysis is obviously magnified when hundreds of cables are involved. Often noise is picked up by circuits

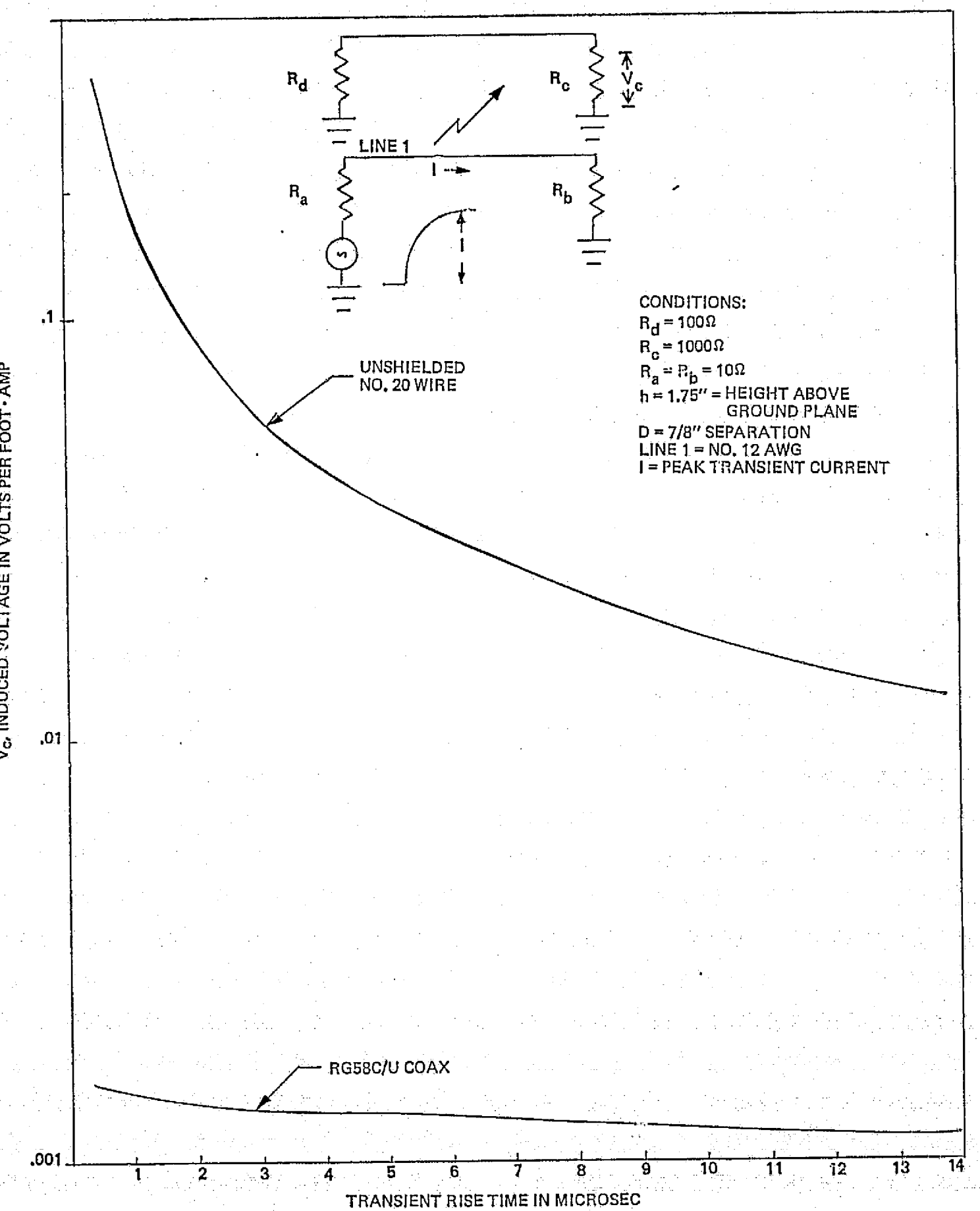


Figure 4-6. Voltage vs Rise Time of Transient Current Input

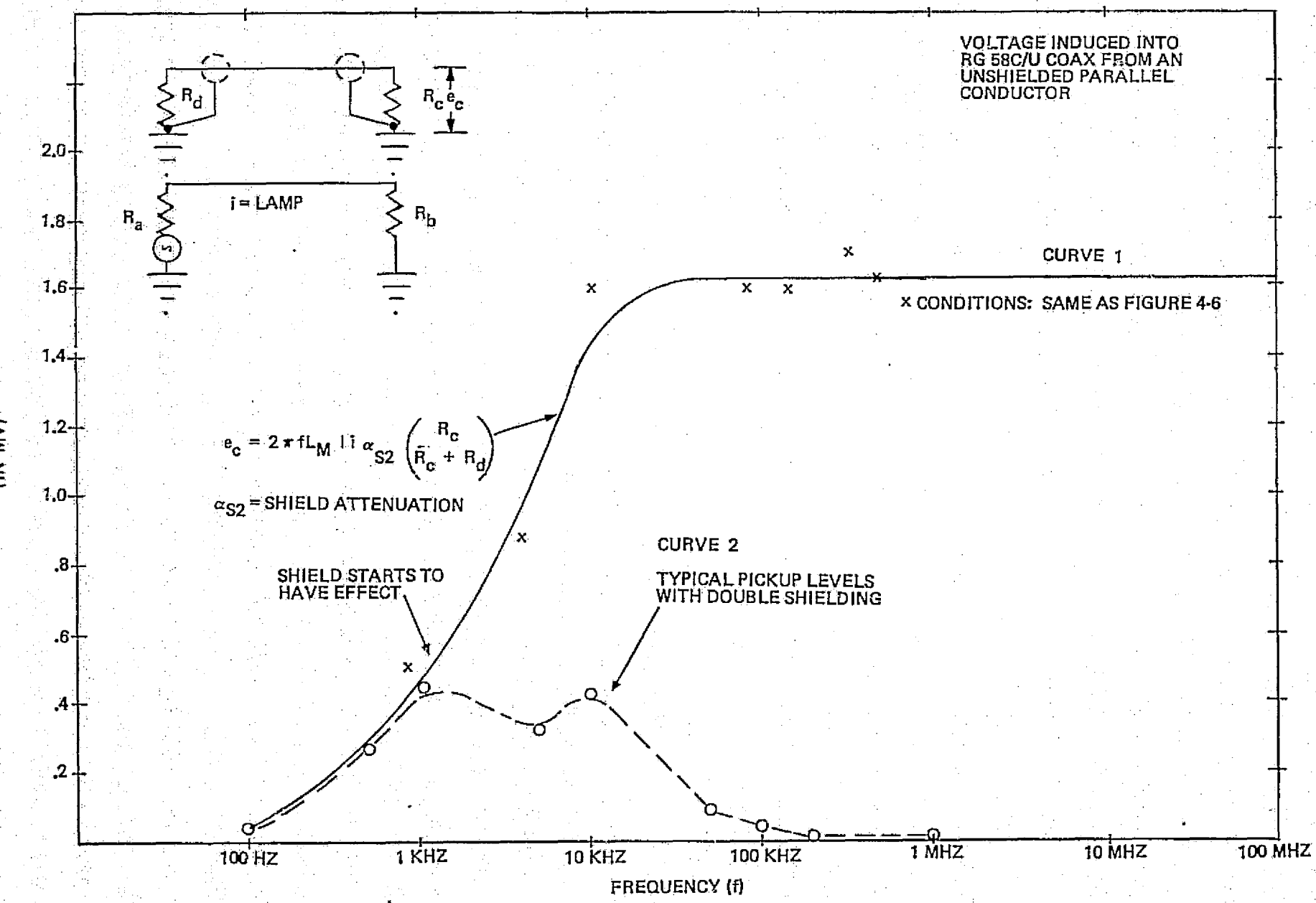


Figure 4-7. Cable Noise vs Frequency

that are inadvertently created by ground connections (ground loops). The subsequent result is that reference ground potentials vary, causing apparent shifts in signals that rely on a common ground reference (single-ended transmission). Since shielding is ineffective at low frequency, good reference ground potentials are difficult to maintain, especially in large vehicles (large areas). Although the SEPS vehicle is relatively small, the high interference levels make it difficult to maintain a good ground reference system. A good reference system should be possible, however, if low impedance ground loops are avoided.

From the above discussion, the following general conclusions and recommendations are proposed:

- o SEPS interfaces should avoid large circuit areas and ground loops. This approach minimizes magnetic field pickup and makes shielding effective.
- o Interfaces should employ balanced receiver devices extensively. This creates configurations similar to circuits #6 to #16 in Figure 4-3.
- o Cables and unit assemblies should employ shields to protect against transient and high frequency noise.
- o On critical, low level, or high accuracy measurements, balanced transmission and reception over twisted shielded cable should be considered.

Specific cabling details and signaling characteristics should be addressed in follow-on Phase B studies.

Driver/Receiver Options

Interface driver/receiver circuits can be classified as one of three types: (1) single-ended (SE), (2) double-ended (DE), or (3) differential (DIFF). Circuits can be linear (analog) or non-linear (logic).

Definitions

Single-ended driver circuits use a ground or other dc level as a reference return. The signal voltage rises relative to this reference and is analogous to on/off binary signals in communication theory. This circuit configuration is generally the simplest and has the lowest failure rate. Signal swing may be either positive or negative with respect to the reference voltage.

Double-ended driver circuits are defined to be dual, single-ended drivers with complementary outputs (i.e., one swings positive while the other swings negative with respect to the other). Double-ended drivers generally do not have a balanced output impedance with respect to ground.

Differential drivers are dual output circuits with lines balanced with respect to ground. Signal voltages on the lines also swing in opposite polarity relative to each other.

Single-ended receiver circuits, which again are the least complex, measure input voltages with respect to a fixed reference. The reference, generally ground, is relative to the receivers power supply system. Input

signal sources accordingly must be connected to the receiver's power supply ground.

Double-ended receiver circuits are dual, single ended receivers.

Differential receivers have differential amplifier input circuitry and provide an output proportional to the potential difference between the two input lines. Differential receivers also exhibit common mode rejection properties.

Practical Interface Options

Figure 4-8 illustrates six candidate driver/receiver pairs. Each is discussed briefly below:

- o Single-ended to Single-ended (SE to SE)

  Although the simplest circuit combination, single-end to single-end transmission schemes require a common ground reference and transfer accuracy is no better than the ground system. Wiring connections are analogous to circuits #1 to #5 of Figure 4-3, which are the most noise sensitive. In addition, the single-ended logic or discrete receiver is a threshold detection device with a fixed threshold. Noise susceptability is established by (1) the accuracy of the signal ground reference, (2) the signal amplitude, and (3) the threshold setting.

- o Single-ended to Differential (SE to DIFF)

  This combination uses the simple unbalanced driver into a balanced differential receiver. The signal at the receiver output is

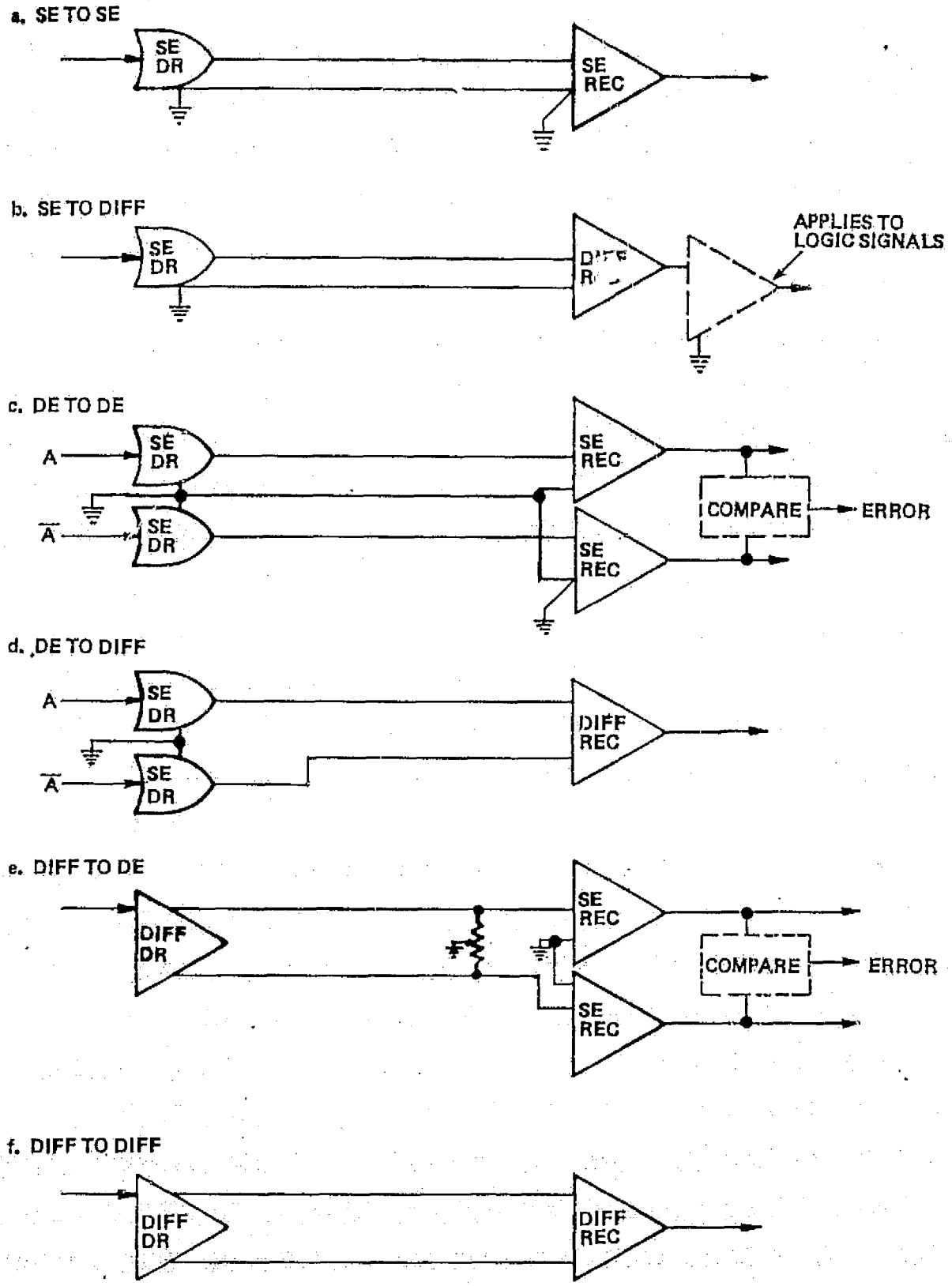


Figure 4-8. Candidate Driver/Receiver Pairs

referenced with respect to the two input lines and, in the ideal case, independent of receiver power supply references. Since the driver is unbalanced, the circuit combination provides little or no common mode rejection. As indicated in Figure 4-8, when used for digital signals, the output of the differential receiver front end will still require a threshold detection circuit.

- Double-ended to Double-ended (DE to DE)

  This configuration could be considered for digital communication. It provides little noise immunity, but it is noise and failure detectable.

- Double-ended to Differential (DE to DIFF)

  This configuration is especially attractive for high rate digital communication. Ground reference shifts appear as common mode and are rejected by the receiver. It also provides common mode rejection to noise coupled onto the transmission cable to an extent determined by driver output impedance balance.

- Differential to Double-ended (DIFF to DE)

  This configuration is similar to the double-ended to double-ended circuit but offers some additional ground reference shift insensitivity.

- Differential to Differential (DIFF to DIFF)

  This is the least noise susceptible and generally involves the most complex circuitry. It provides high common mode rejection against both ground reference and externally coupled noise.

Isolation

Electrical isolation techniques can be used with the interface circuit options. Isolation schemes utilize transformers, light emitting diodes or relays. Isolators will eliminate requirements for a ground reference and tend to make drivers and receivers act as differential devices.

Table 4-4 provides a summary of signal method comparison. The table illustrates that no one method is best for all signal applications.

Failure Isolation Options

Standby sparing redundancy is planned for the I/O. Effective redundancy management dictates that any single failure in a function should not prevent the spare unit from operating. Since at least dual redundant input/output sections are required, all interfaces with the I/O will involve failure tolerance considerations. In some instances, redundant sources and output sinks are also involved.

Implementation of redundancy can employ cross-strapping or single-string approaches with cross-strapping generally providing highest reliability. However, cross-strapping also places the greatest demand on redundancy management and design detail. Failure isolation considerations discussed here apply to cross-strap applications.

Table 4-4. Signal Method Comparison

	IN BAND NOISE REJECTION	CMR (TYPICAL)	SYSTEM NOISE SUSCEPT	PWR DISS	RELIABILITY	COST/ SIZE
1. SE to SE	($\lesssim$ Th) 1	(0) 1	1	3	3	3
2. SE to DIFF	($\lesssim$ Th) 1	(0) 1	2	2	2	2 1/2
3. DE to DE	($\lesssim$ Th) 1	$\left(\frac{\text{Detects}}{\text{CM}}\right)_2$	2	2	2	2
4. DE to DIFF	(V_s) 2	(>0) 1 1/2	2 1/2	2	2	2
5. DIFF to DE	(V_s) 2	$\left(\frac{\text{Detects}}{\text{CM}}\right)_2$	2 1/2	1	1	1
6. DIFF to DIFF	(V_s) 3	(> 40db)3	3	1	1	1

LEGEND:

RELATIVE RATINGS: 3 IS BEST, 1 IS LEAST ATTRACTIVE

$\lesssim$ = LESS THAN BUT APPROXIMATELY EQUAL TO
Th = THRESHOLD VOLTAGE WHICH DEPENDS ON SIGNAL AMPLITUDE
V_S = SIGNAL VOLTAGE
CM = COMMON MODE NOISE
CMR = COMMON MODE REJECTION

Practical isolation options include the following:

- o Active Isolation - dual output drivers and/or receivers are employed.
- o Resistor Isolation - when loading effects such as shorts permit, resistive isolation is often the most economical.
- o Diode Isolation - logic signal with unidirectional current flow can use diodes to isolate electrical short failures. Diode isolation usually requires powering-down the unused spare.
- o Field Effect Transistor (FET) Isolation - FETs can be used for linear signals and low level logic if impedances permit.

Combinations of the above are candidates for the SEPS I/O design with the best method determined by the signal characteristics, criticality and transfer accuracy.

Recommended SEPS Interface Design

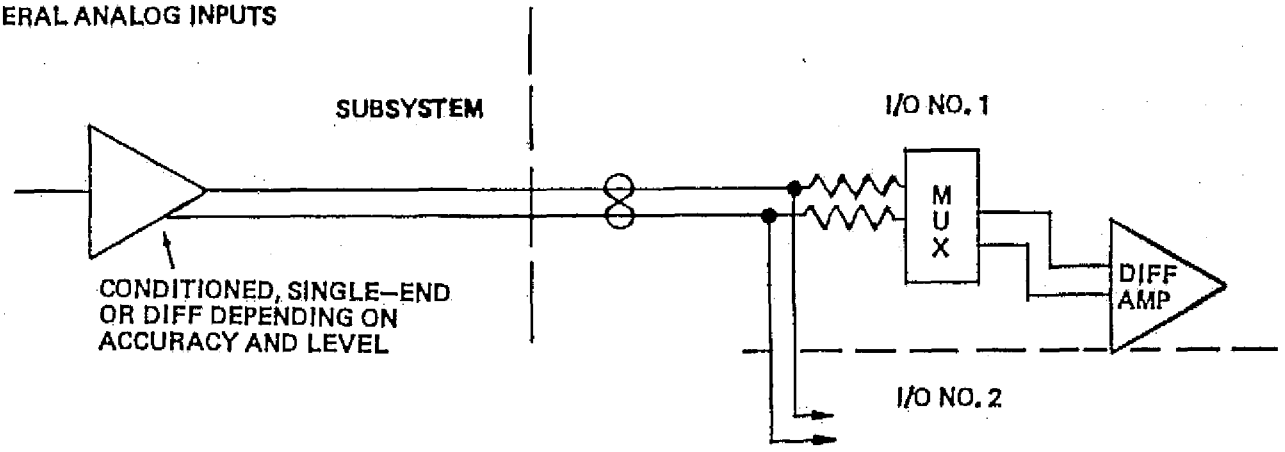
Input Signals

Figure 4-9 summarizes the recommended configurations for redundant signal input interfaces to the I/O. Most of the various signal types anticipated for SEPS are included. Specific signal handling treatment will be required in the generation of hardware specifications.

Output Signals

Figure 4-10 summarizes recommended the configurations for redundant CCS outputs.

1. GENERAL ANALOG INPUTS



2. TEMPERATURE/PRESSURE/POTS (SINGLE STRING RECOMMENDED WHERE PRACTICAL)

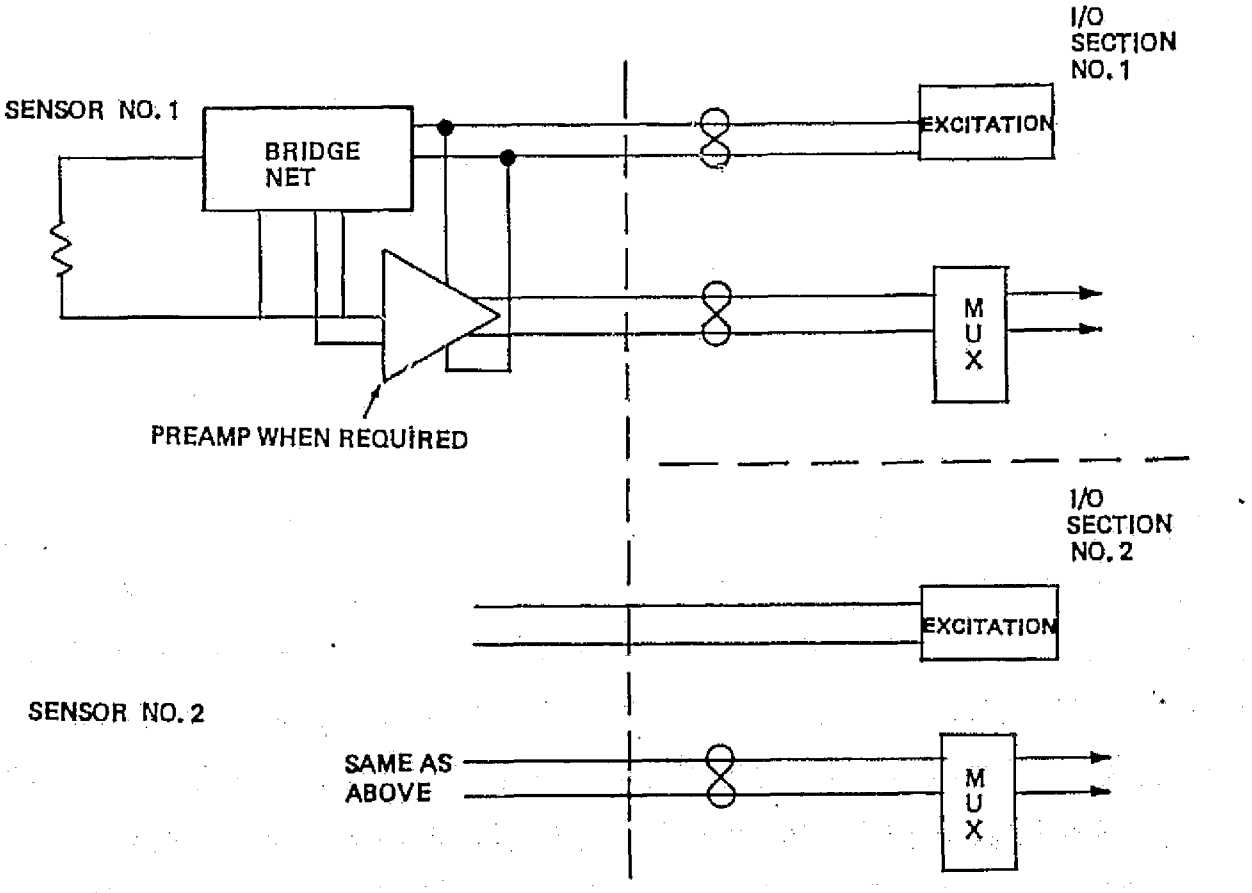
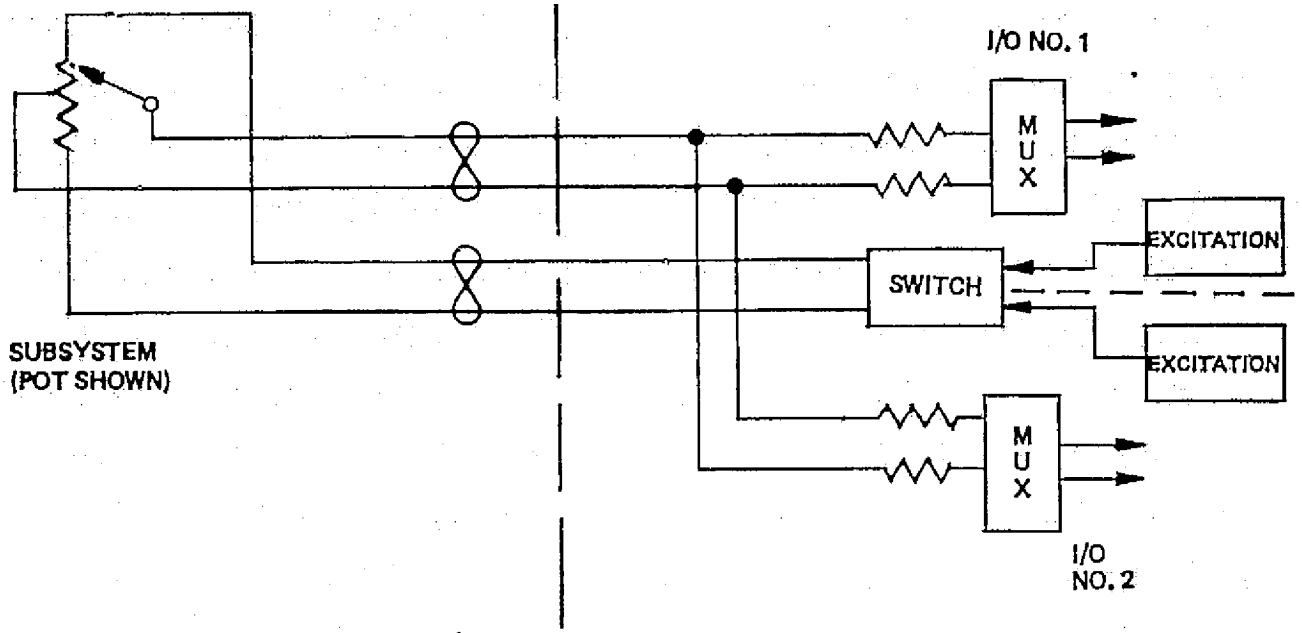
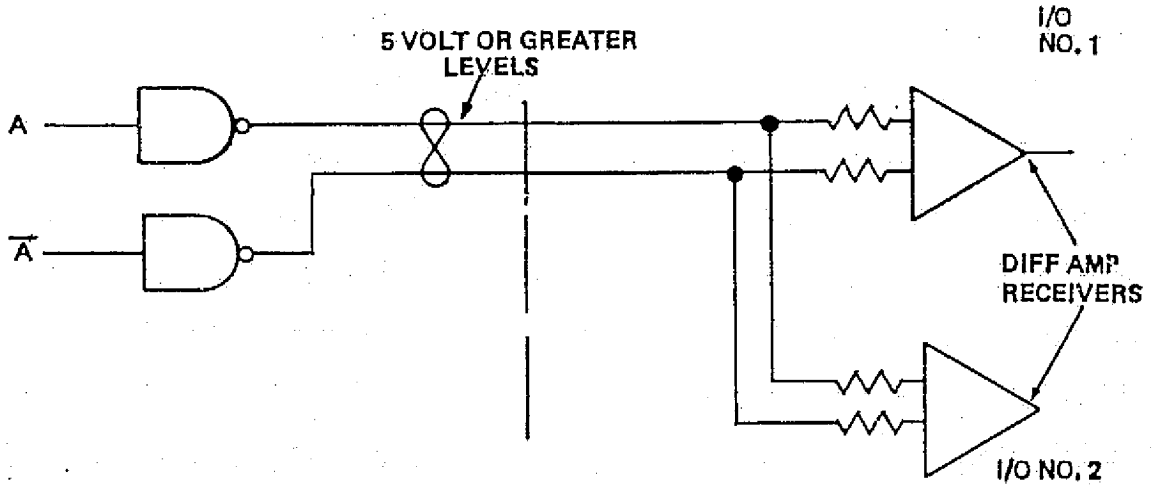


Figure 4-9. Recommended Input Interface Concepts

3. SIMPLEX TEMPERATURE/PRESSURE/POTS



4. SERIAL LOGIC



5. DISCRETES (PRELIMINARY)

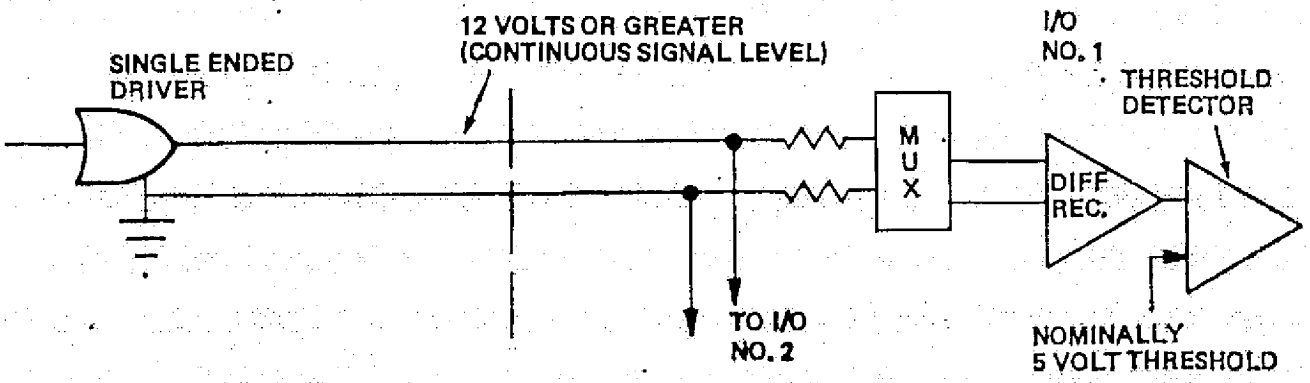


Figure 4-9. Recommended Input Interface Concepts (Cont)

6. SWITCH CLOSURE

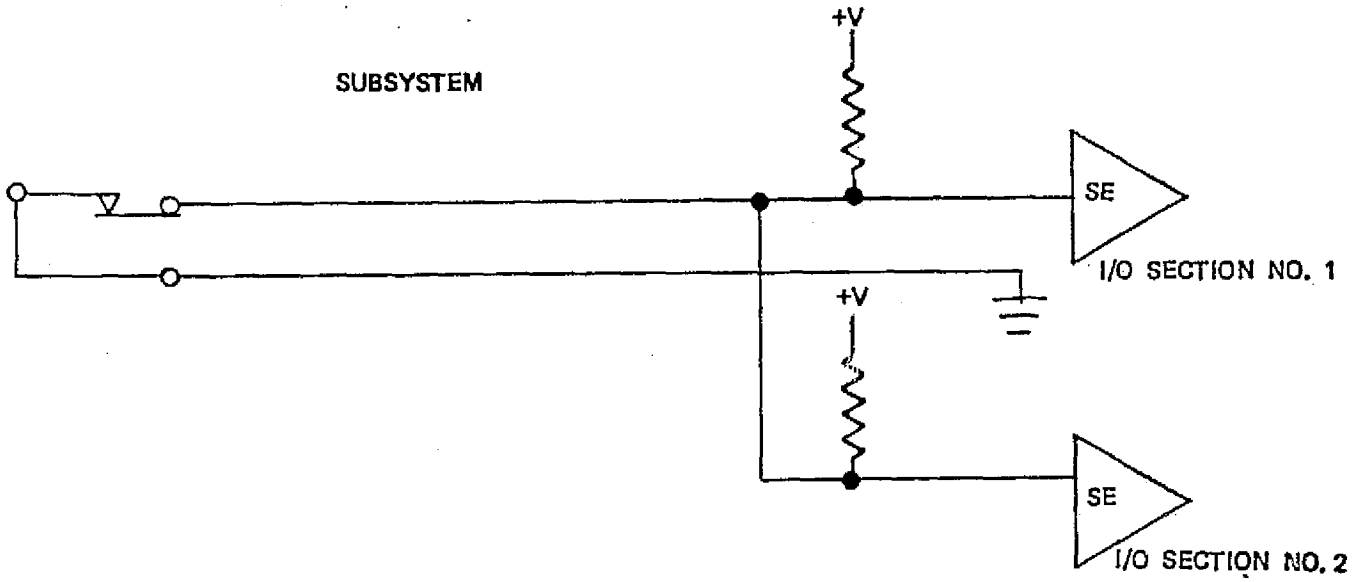


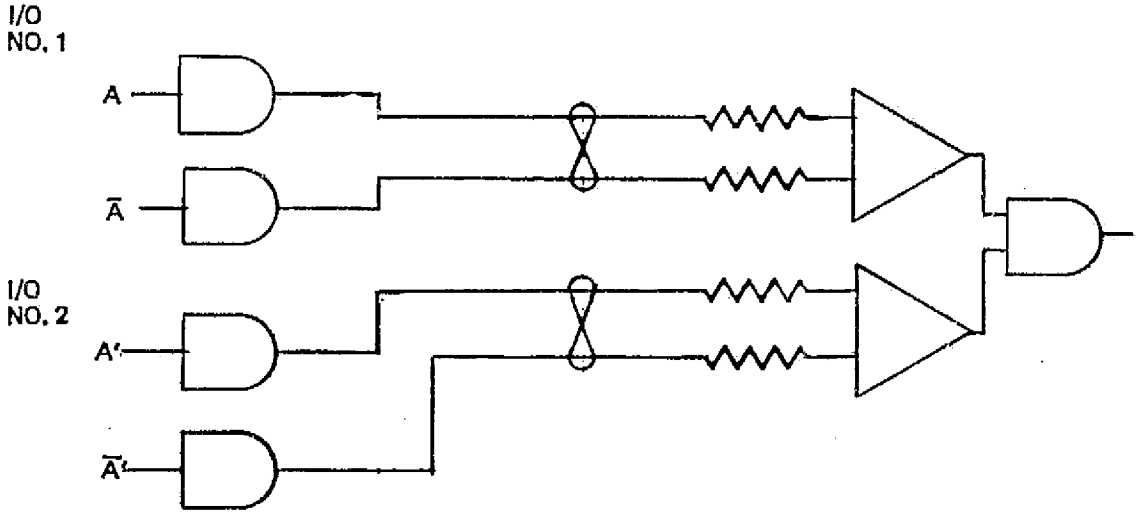
Figure 4-9. Recommended Input Interface Concepts (Cont)

NOTE: SIMPLEX SUBSYSTEMS SHOWN USE ISOLATION RESISTORS FOR CROSS STRAPPED REDUNDANT SUBSYSTEM CONNECTIONS.

1. ANALOG

NO ANALOG OUTPUT REQUIREMENTS HAVE BEEN IDENTIFIED FOR SEPS

2. SERIAL DIGITAL & TIMING



3. DISCRETES TO RELAYS & ISOLATED LOADS

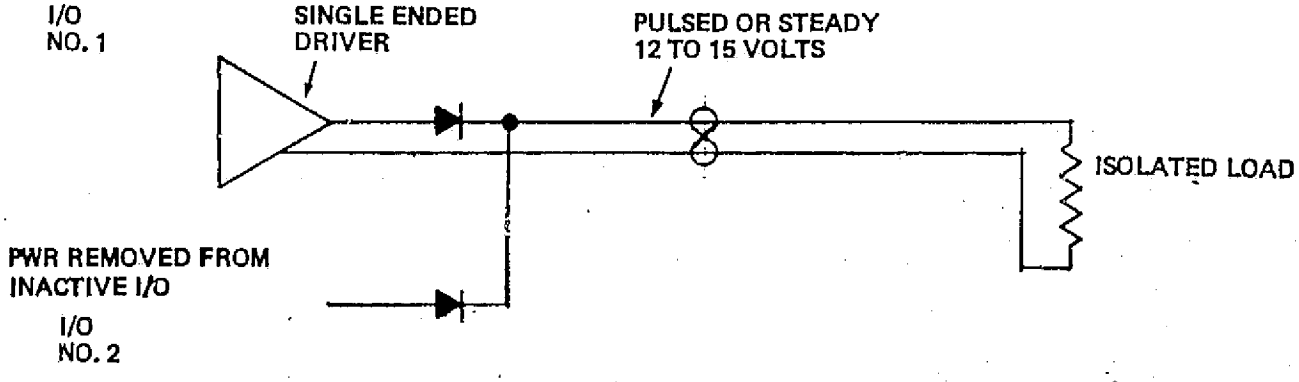


Figure 4-10. Recommended Output Interface Concepts

4. DISCRETES TO NON-ISOLATED LOADS

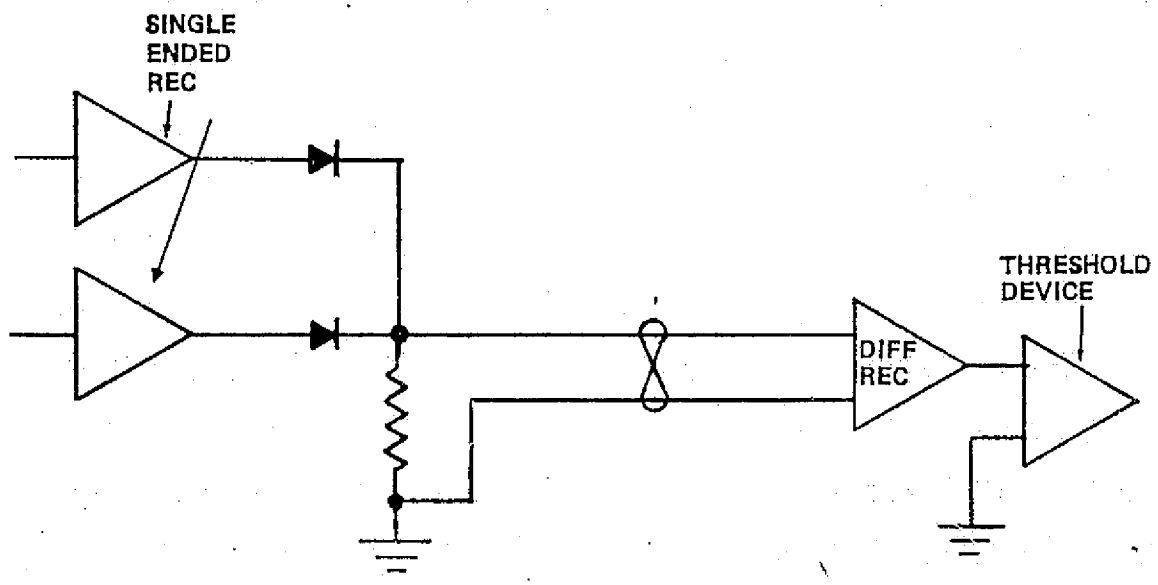


Figure 4-10. Recommended Output Interface Concepts (Cont)

Recommendations include consideration for EMI, as discussed previously, as well as failure isolation. The treatment is general and accordingly each signal interface definition will require a review of all trade considerations in follow-on Phase B studies.

4.2.3.3 Recommended I/O Design

The recommended I/O design is a hybrid design utilizing a centralized I/O with two remote acquisition units to handle high density signals to and from the solar array and propulsion subsystems. The I/O contains redundant input circuitry, output circuitry, I/O timing and control, command interface, and data handling circuitry. A block diagram of one-half of the custom I/O section is shown in Figure 4-11, and Figure 4-1 shows the overall I/O block diagram.

The basic I/O design utilizes the common parallel input and output data bus concept. Data flow from the CPU to the I/O is accomplished via a 17-bit output bus which transmits both address and data on a time-shared basis. The I/O timing and control circuitry checks parity of the incoming data, decodes the I/O address, gates the data onto the output bus and generates a load strobe to the selected output register. Input data to the I/O is conditioned or converted (in the case of analogs), then gated onto the input bus to be read by the CPU. In the case of a read command, the timing and control circuitry checks parity of the command word (address) from the CPU, decodes the command, issues a strobe pulse to gate the data onto the I/O input bus, generates a parity bit, and gates the I/O input data to the CPU. In the case of both a read and write command, the I/O timing and control circuitry generates all "handshaking" commands necessary to interface with the CPU.

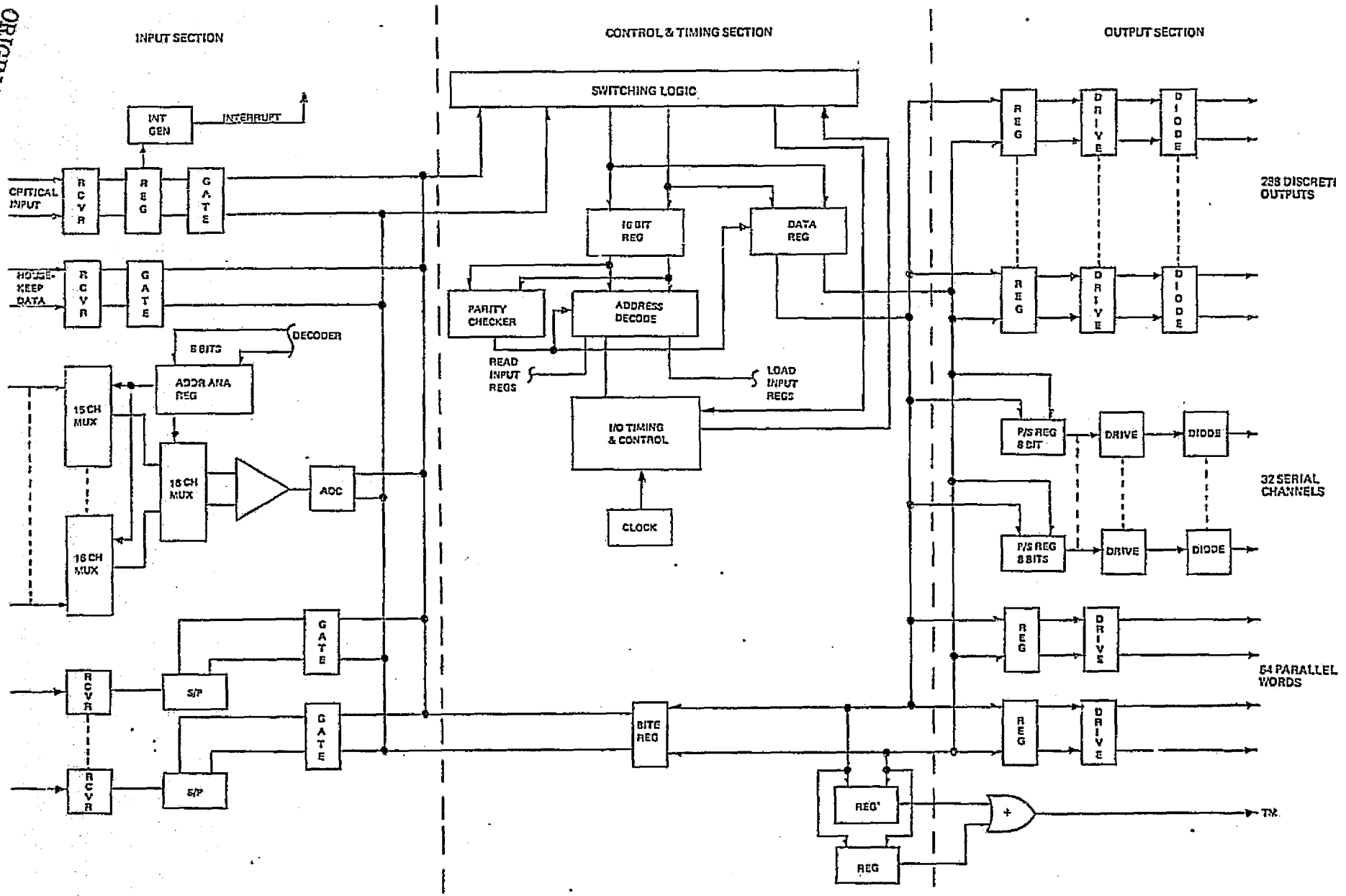


Figure 4-11. One-Half Custom I/O Section Block Diagram

The I/O provides the interface between the telemetry buffer, located in main storage, and the tape recorder or TM transmitter. The CPU collects TM data from I/O inputs, stores this data in the TM buffer in main storage; then when the buffer is full, the data is read to the tape recorder or TM downlink. The I/O provides all timing and control signals to the tape recorder or TM transmitter to perform this operation.

The design of the I/O section is divided into three major categories: Input Circuitry, Output Circuitry, and Timing and Control Circuitry. Each of these is discussed in detail below.

4.2.3.3.1 I/O Input Circuitry

The custom I/O input circuitry is divided into the following categories: critical discretes, housekeeping discretes, parallel digital words, serial digital words, and analog inputs. Storage will be provided for [illegible]put types with the exception of housekeeping discretes.

A typical group of critical discrete inputs is shown in Figure 4-12. The output of the receiver circuit is connected to the clock input of a D flip-flop; the D input of the flip-flop is connected to a logic level "one". The leading edge of the discrete input will clock a "one" into the storage cell. The Q side of the flip-flop is connected to a 16-input NAND gate to generate an interrupt level to the CPU. The level of interrupt will dictate to the CPU which input channel is to be serviced. Following a read command from the CPU, the I/O timing and control circuitry will issue a clear command to the channel, which will reset all of the 16 bits of the discrete input group.

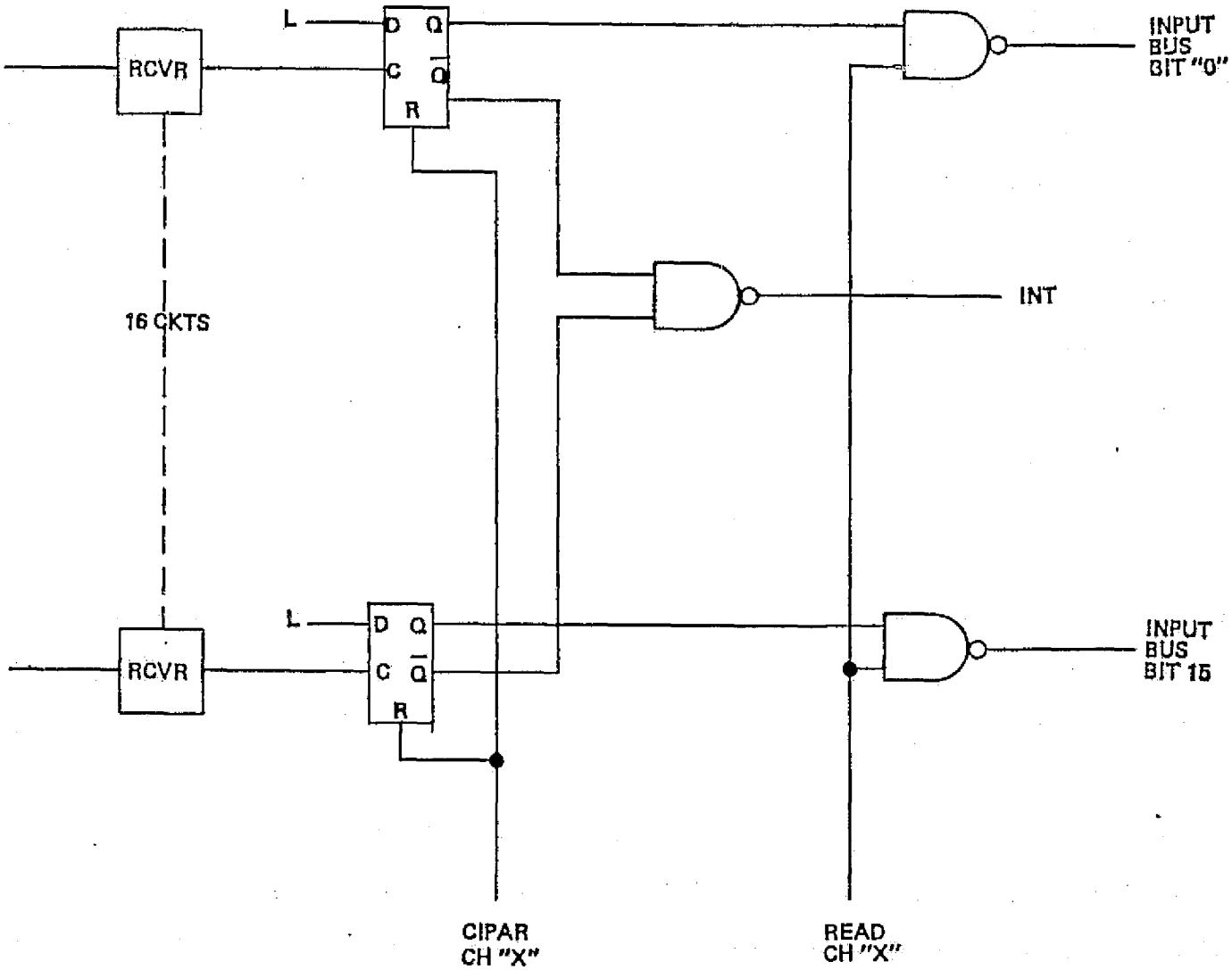


Figure 4-12. Critical Discrete Input Circuitry

Critical discretes will be grouped into 16-bit patterns. This is done to facilitate the reading of the discretes onto the I/O 16-bit input bus. Each group of 16 bits will generate a unique interrupt level to the CPU.

Housekeeping discretes will not be provided with storage elements in the I/O. These discretes will be polled at a regular interval dictated by the program resident in main memory. These discretes will also be grouped into 16-bit patterns as were the critical discretes. The grouping will be done with respect to the sampling rate of the discretes. The housekeeping discretes will be buffered by a receiving circuit and gated onto the input bus by a decoded read command from the I/O timing and control circuitry.

Parallel digital words transmitted from a subsystem to the I/O will not be stored in the I/O if storage for that word is provided in the subsystem. If no storage is provided in the subsystem, the parallel word will be loaded into a parallel/parallel register in the I/O. A block diagram of a typical parallel word from a SEPS subsystem to the I/O is shown in Figure 4-13. As was the case with critical discrete inputs, critical digital words will generate an interrupt to the CPU. A decoded read command from the I/O timing and control logic will gate the stored data onto the input bus. Non-critical or housekeeping words will be polled by the CPU at a predetermined rate.

Serial digital data received by the I/O will be loaded into a serial to parallel register, as shown in Figure 4-14. The CPU will read the parallel output by issuing a read command for that data channel. There are three possible methods of clocking the serial data from the subsystem to the I/O:

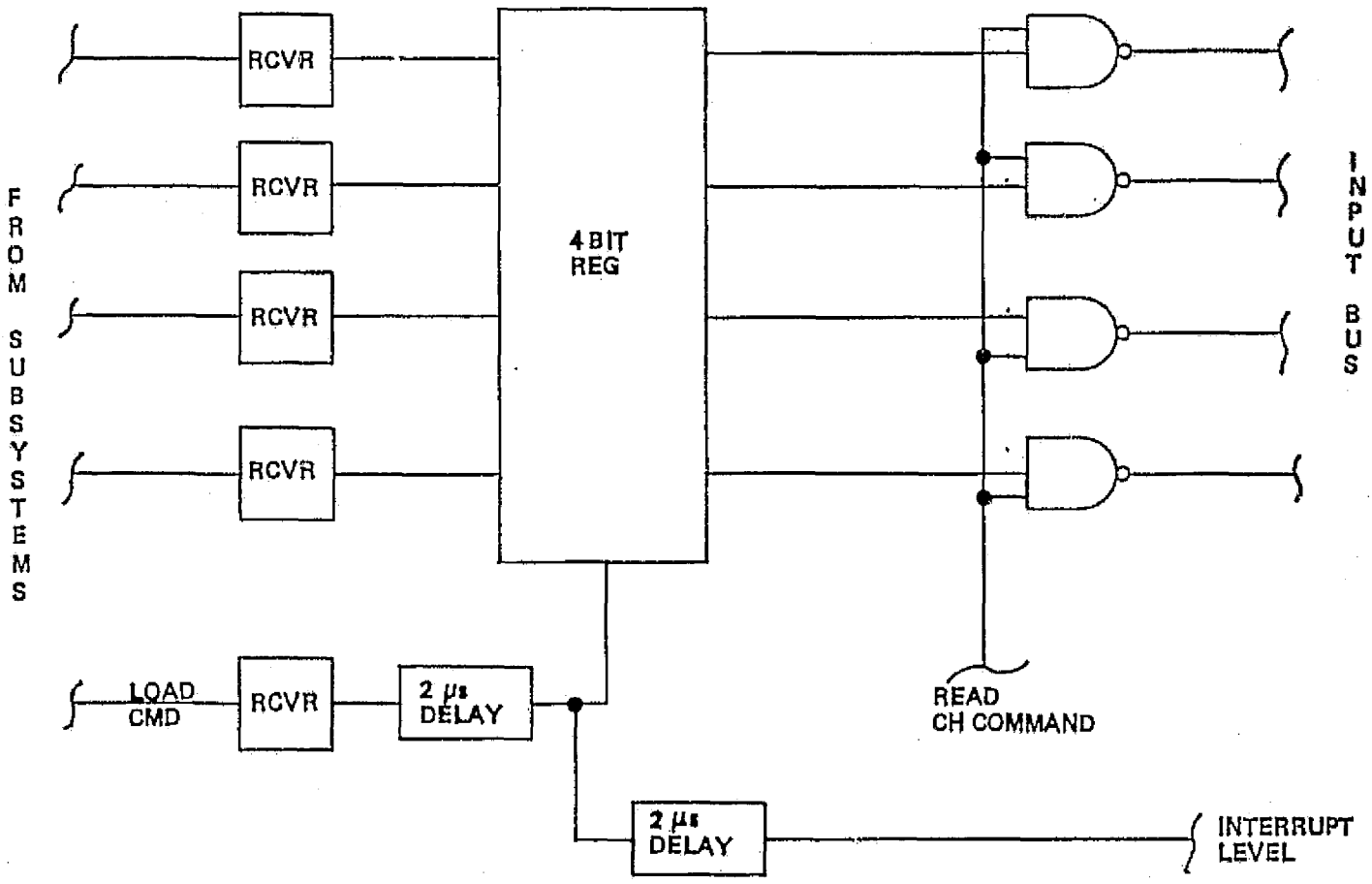


Figure 4-13. Parallel Digital Word Input Circuitry

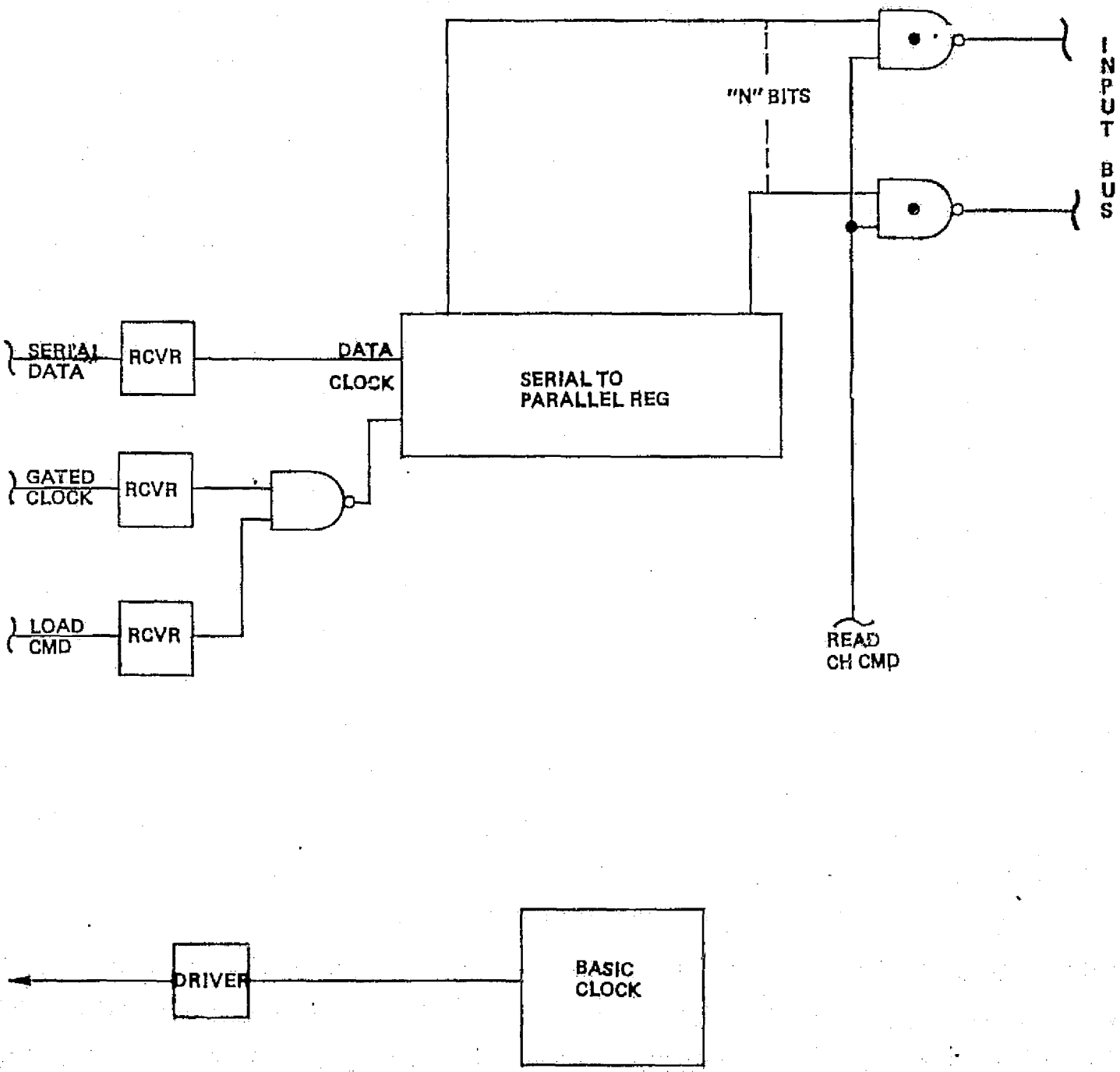


Figure 4-14. Serial Digital Word Input Circuitry

1) The subsystem could generate and supply the load command and the clock to the I/O; 2) The I/O could supply the clock to the subsystem for clocking; 3) The subsystem could generate a self-clocking code such as Manchester II. At the present time the best in terms of simplicity, reliability, power and volume is item (1). This scheme is shown in Figure 4-14.

The relatively high number of analog inputs dictates the use of a two-level analog multiplexer. A block diagram of the I/O analog input multiplexer is shown in Figure 4-15. A two-level analog multiplexing scheme will be used to receive and process analog inputs to the custom I/O. This will allow the multiplexing of up to 256 single ended analog inputs or 128 double ended analog inputs.

The first level of multiplexing consists of up to 16 16-input mux circuits. The subsystem analog inputs are connected to the inputs of these multiplexers. The outputs of each of the first level multiplexers (16 of 256) are connected to one of the 16-input channels of the second level mux. The output of the second level mux (1 of 256) is connected to the input of a buffer circuit for impedance matching and error reduction. The output of the buffer circuit is connected to the input of the A/D converter. The converted analog channel is gated onto the input bus to the CPU in the same manner as the discrete inputs.

The analog address register receives eight bits of analog address from the I/O timing and control section for each analog channel to be read by the CPU. This address is broken into two four-bit address codes. The four low

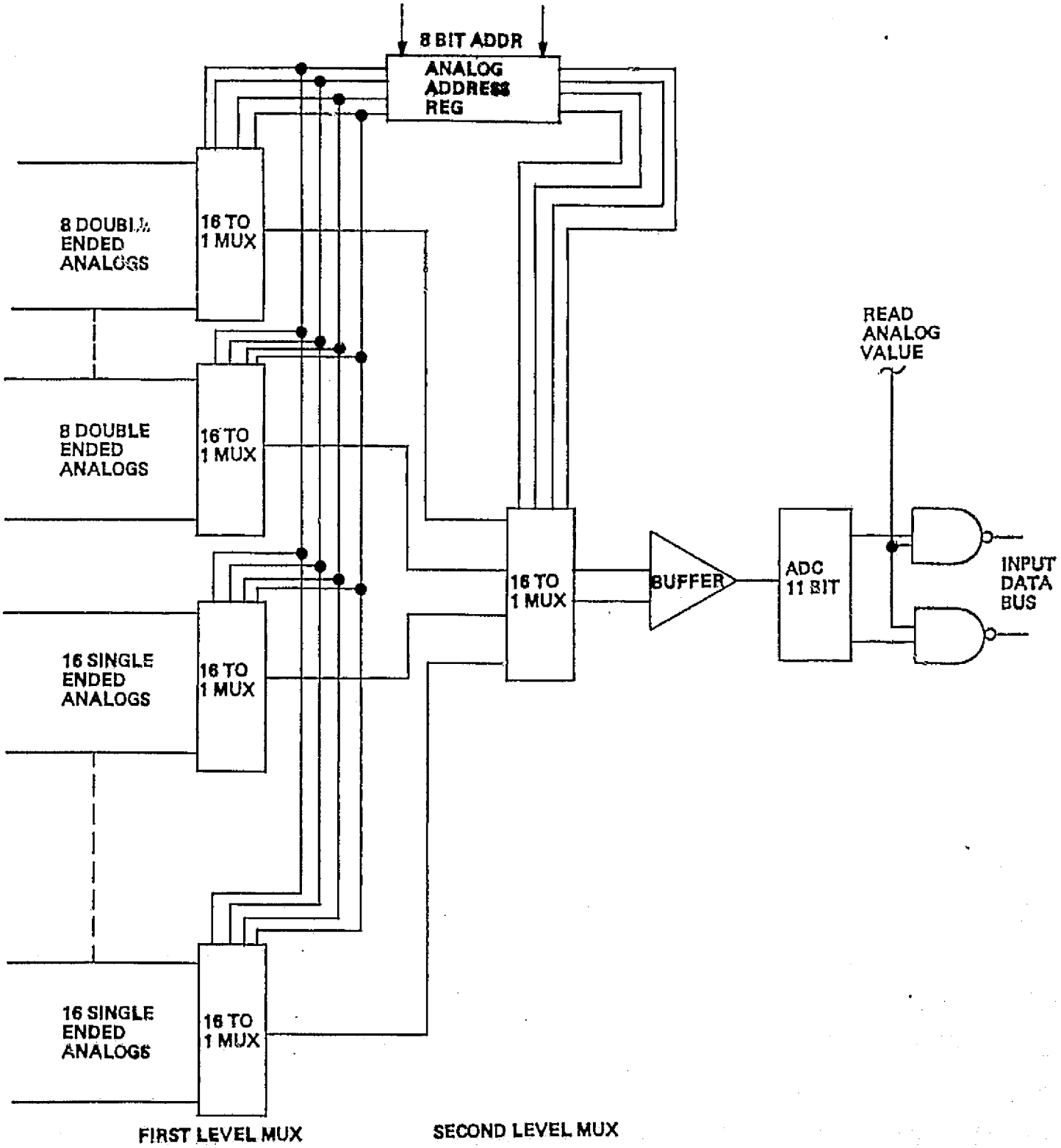


Figure 4-15. Input Analog Multiplexer Circuitry

order bits select one of the sixteen inputs at each of the first level mux's; the four high order bits select one of sixteen inputs of the second level mux (i.e., the high order bits select the output of one of the first level mux's) to be routed to the A/D converter for conversion.

4.2.3 3.2 I/O Output Circuitry

The custom I/O will provide discrete, serial digital and parallel digital word outputs to various SEPS subsystems. These outputs will be controlled by the CPU. In order to perform this function, the I/O will receive from the CPU a command, a write address, and 16 bits of data. The I/O is structured such that the 16 data bits will be set onto a common 16-bit parallel output bus; the decoded address will then be used to gate and strobe the data into the proper output register. All discrete outputs will be high level (+28 Vdc) capable of driving the specified subsystem load impedance. Serial and parallel output words will be TTL compatible.

A simplified block diagram of a group of high level discrete outputs is shown in Figure 4-16. The data which appears on the I/O output bus will be strobed into a 16-bit holding register by a decoded load command generated by the I/O timing and control circuitry. If the discrete to be issued is of the pulsed type, the load command will also start the pulse generation circuitry, which is a counter set to generate a pulse of specified duration. The output of the pulse generation circuitry is ANDed with the output of the output register. The output of the AND gate will control the high level driver (shown as an NPN transistor), turning ON for the length of time set by the pulse circuitry. Isolation diodes are connected in series with the output to provide failure protection for both halves of the redundant I/O section.

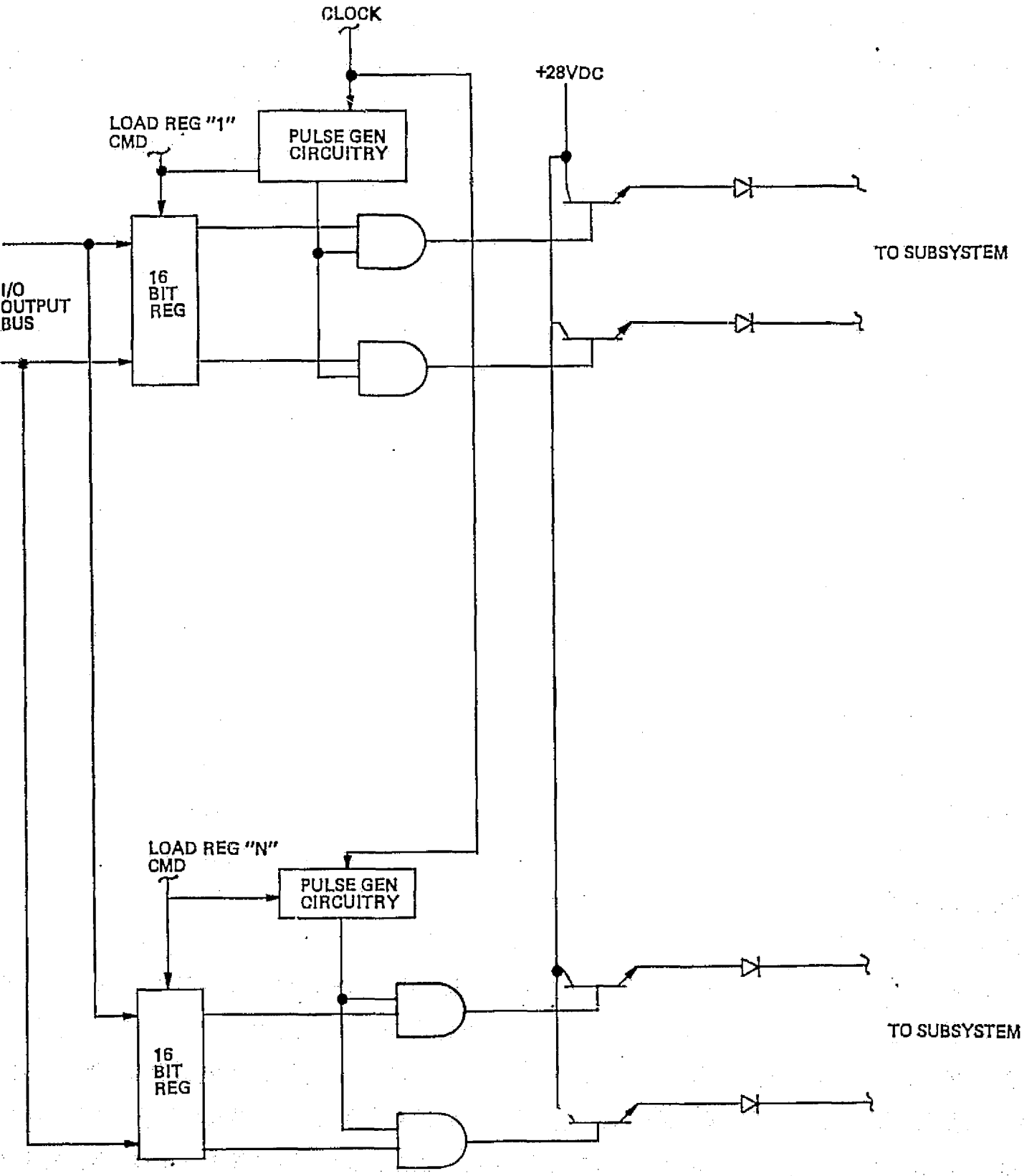


Figure 4-16. High Level Discrete Output Circuitry

Serial and parallel digital outputs of the I/O are shown in Figure 4-17.

Serial outputs are generated when the I/O receives a write command from the CPU for a specific serial word. That word is loaded parallel into a parallel to serial register. The data is then clocked serially to the subsystem. The clock is also routed to the subsystem where it may be used to clock in the serial word. Parallel digital outputs are simply loaded into a holding register by the I/O timing and control circuitry and presented to the receiving subsystem through drivers.

4.2.3.3.3 I/O Timing and Control Circuitry

The I/O timing and control circuitry provides all timing signals, load and control signals, data routing, address decoding, parity generation and checking and generation of all "handshaking" signals with the CPU. The I/O will be power cycled in order to conserve power when a particular function is not in use. However, the control circuitry which interfaces with the CPU and the critical discrete inputs are in a powered state at all times. A block diagram of the timing and control section is shown in Figure 4-18.

Communication between the CPU and the I/O is accomplished via a 17-bit output bus (IOBO), a 17-bit input bus (IOBI) and seven "handshaking" control lines. Primary communication to and from the I/O is accomplished by the Direct Out and Direct In sequences.

Write Sequence

To load data into an I/O discrete output channel, parallel digital word, channel, or serial digital output channel, the Direct Out sequence is followed. This sequence is shown in Figure 4-19. In this figure, negative

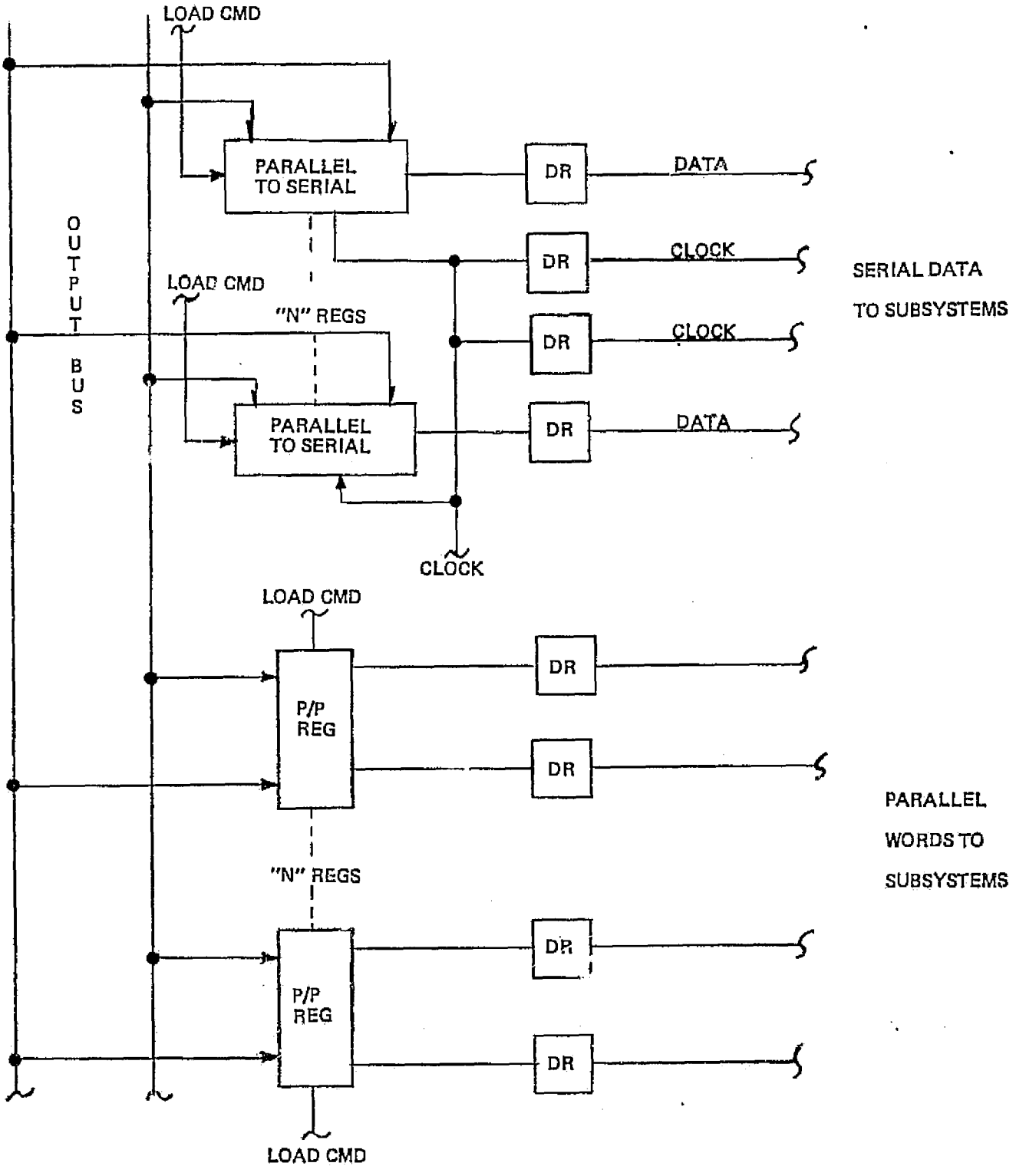


Figure 4-17. Digital Word Output Circuitry

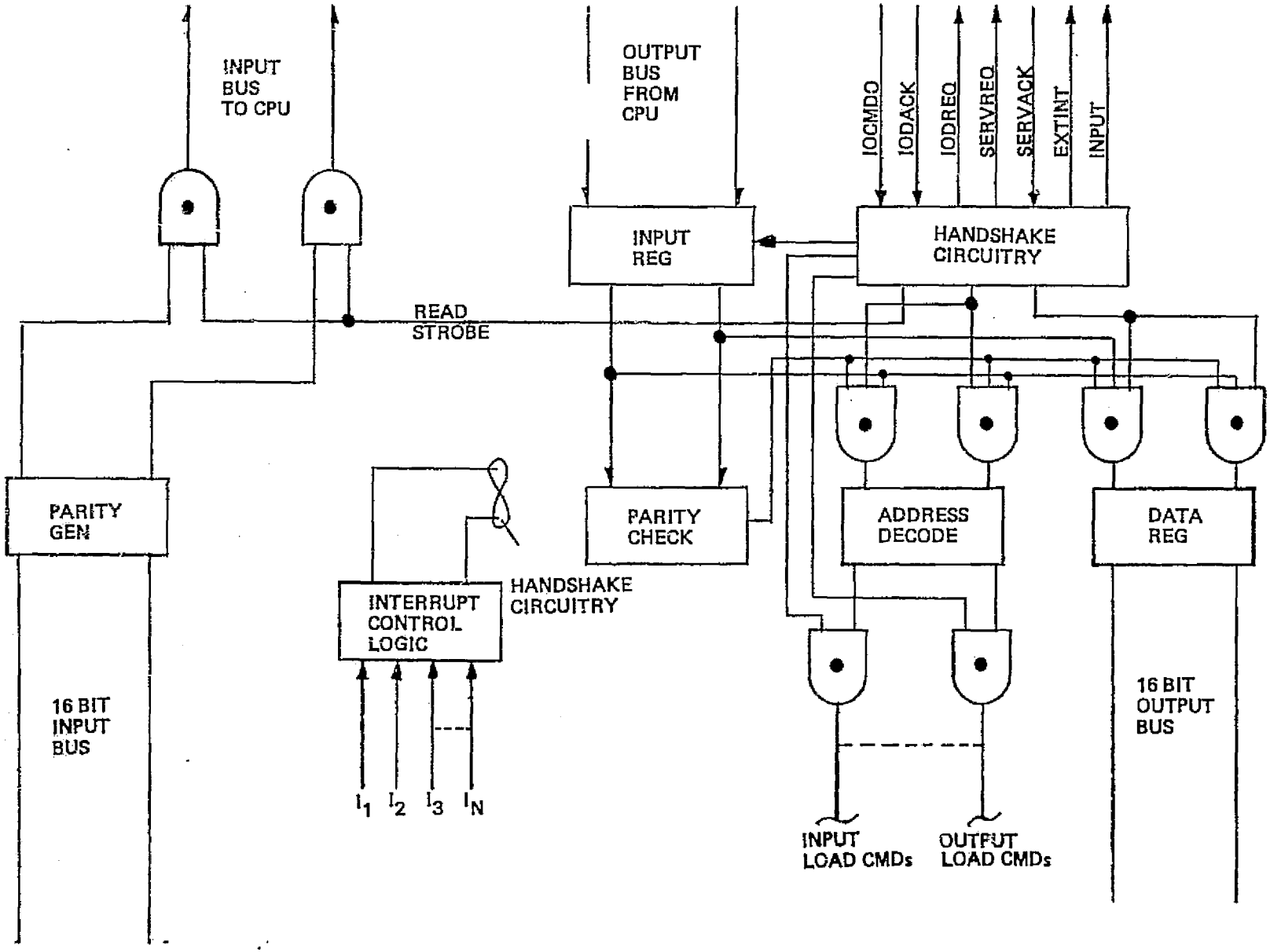


Figure 4-18. I/O Timing and Control Section Circuitry

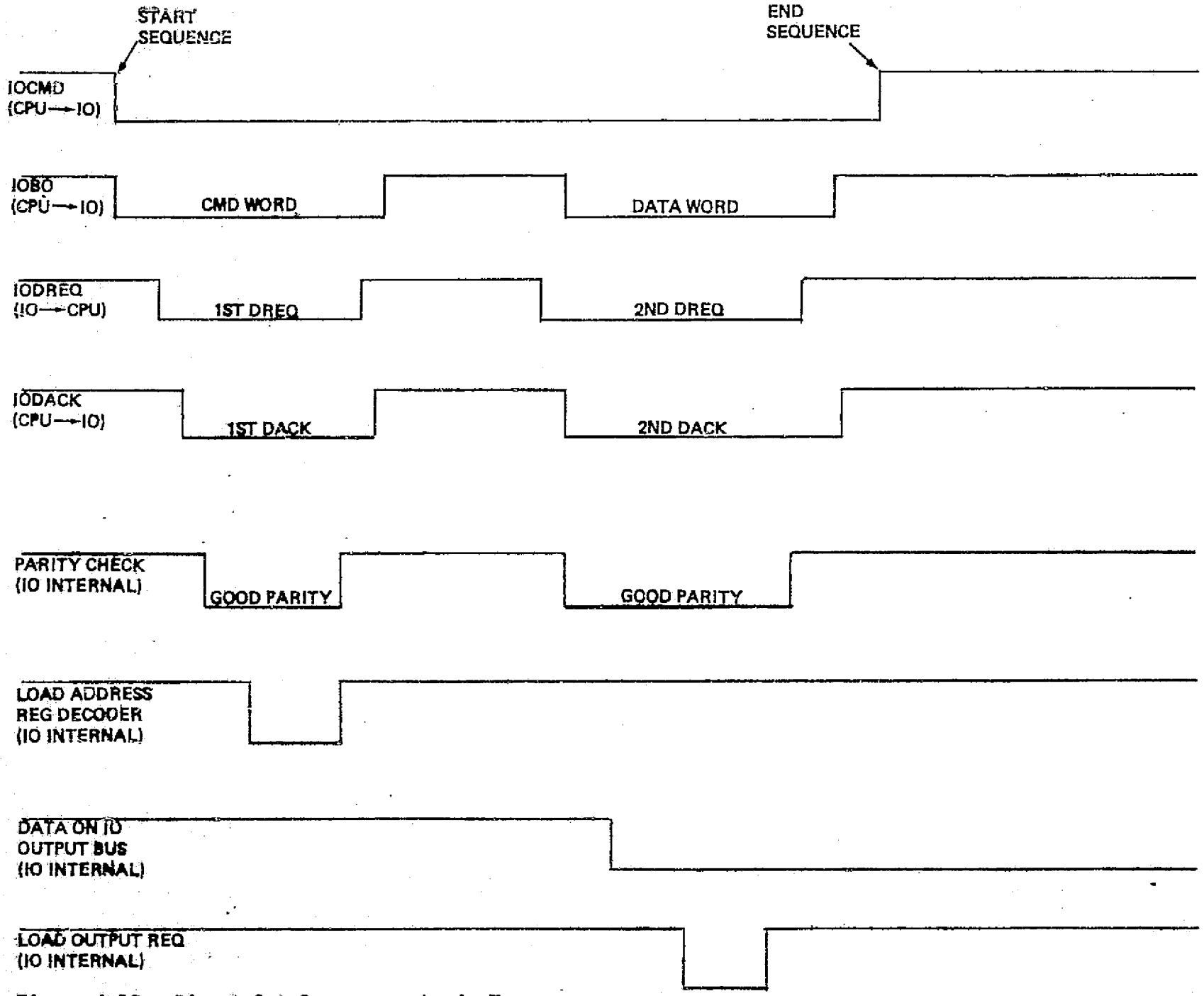


Figure 4-19. Direct Out Sequence - Logic True

levels are active and a sequence of events is depicted rather than actual time intervals.

To start a write operation to the I/O, the CPU issues the IOCMD command and places the I/O register address on the I/O output bus (IOBO) line simultaneously. The I/O will issue a data request signal (IODREQ) to the CPU which tells the CPU that the command was received. The information on the IOBO lines is parity checked and parity is stripped; if parity is good, the sixteen data bits are loaded into the I/O address register. The address information is decoded and gate conditions are set (Read/Write, DO/DI, channel number, etc.).

The DREQ line is then deactivated, signifying the completion of the first word transfer. Following delays and settle time, the DREQ line is activated by the I/O, starting the second word transfer. The second word is the data word which is parity checked, stripped, and placed onto the I/O output bus. Following a small delay, the timing and control logic generates a LOAD OUTPUT strobe which is ANDed with the decoder gates to generate a load pulse to one unique I/O output register. The sequence is then terminated by the I/O deactivation of the second DREQ signal.

Read Sequence

To read data from the I/O discrete inputs, analog inputs, serial and parallel inputs the Direct In sequence will be followed. This sequence is shown in Figure 4-20. The CPU starts the sequence with simultaneous issuance of IOCMD and the seventeen bit parallel word which designates the I/O input channel address that the CPU wants to read. Parity is checked and

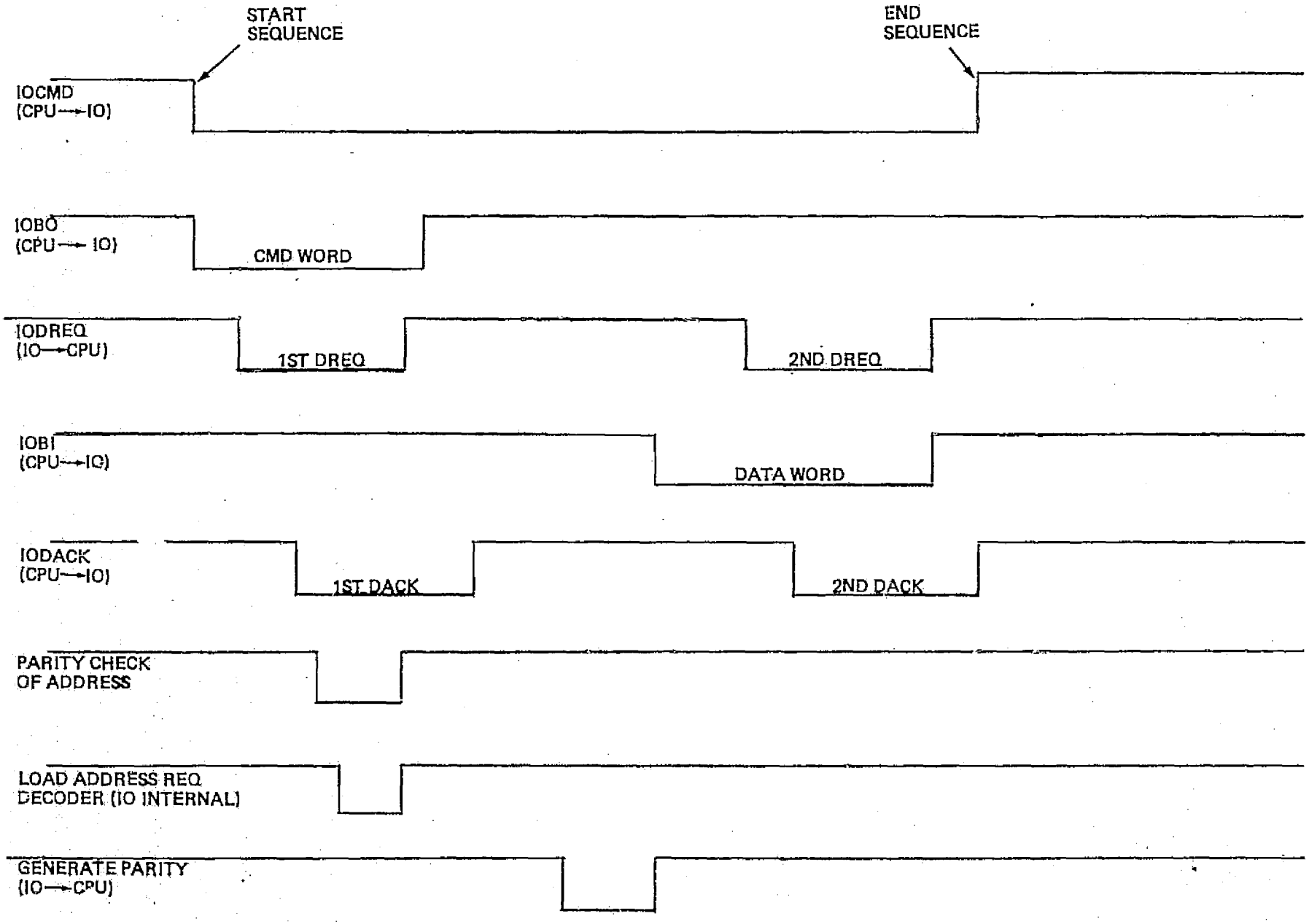


Figure 4-20. Direct In Sequence - Logic True

stripped, and the command word is decoded. Decode gates are conditioned to allow the strobing of the selected word onto the I/O input bus. In the case of the analog inputs, the analog address register is loaded with eight bits which will select the proper analog channel to be routed to the I/O converter.

The handshaking sequence for a Direct In sequence is the same as that for a Direct Out except the second word (data word) is on the input bus lines and parity is generated for this word in the I/O.

The formatting and bit allocation for both the Direct In and Direct Out sequence are shown in Figure 4-21.

Critical Input and Telemetry Readout

When a critical input is received by the I/O, the input circuitry will generate an interrupt which is unique to that input group. The I/O timing and control circuitry will store this interrupt, generate a code word, and generate the necessary interrupt handshaking signals to the CPU. When the CPU receives an interrupt, it will perform a Direct In sequence to read the critical input register. Following this operation, the I/O interrupt register will be cleared unless another interrupt has been received during the servicing of the first interrupt. In that case, the next interrupt will be processed.

The telemetry buffer will be located in main storage for the baseline SEPS design. Therefore, TM data will be accumulated by polling TM channels and loading (via Direct In sequence) into the allocated 4K word buffer. In

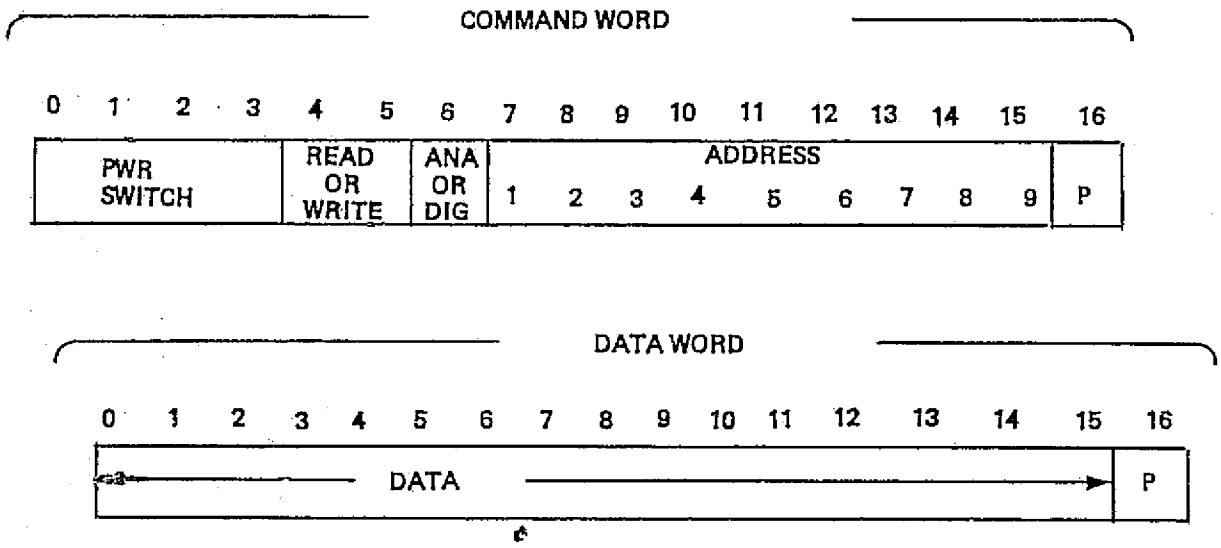


Figure 4-21. Direct In/Direct Out Format and Bit Allocation

order to read this data out to either the tape recorder or the TM transmitter, a sequence called Buffered I/O will be performed. In this sequence, the CPU will, when the buffer is full, issue to the I/O an address command followed by a sequential reading of the buffer. The I/O will alternately parallel load and then serial output the buffer data at a 32 kbps rate to the tape recorder or TM down link at a 1 kbps data rate. The transfer of buffer data is under the control of the CPU.

Power Switching

In order to conserve power, the I/O will employ power switching. The spare I/O will be completely powered down, but the operating I/O will power only the section of the I/O which is being used. The timing and control section and the critical inputs will be powered at all times. The discrete outputs, serial outputs, parallel outputs, telemetry outputs, analog inputs, serial inputs and housekeeping discretes will be power cycled to conserve power.

Error Detection

The custom I/O will employ a BITE register, parity bits and feedback to detect equipment malfunctions.

As previously stated in this section, word transfer between the CPU and I/O will contain a parity bit. Odd parity will be checked by the I/O before any function is performed. Should a parity error be detected, an interrupt will be issued to the CPU by the I/O.

A BITE register will be provided in the I/O design to check bus transfer. The BITE register will be loaded by a Direct Out sequence. The BITE register is then read by a Direct In sequence. This will serve to check both the I/O input and output buses, I/O timing, I/O parity and some I/O decoding circuitry.

It is recommended that certain output signals from the I/O be functionally wrapped to an I/O input to provide end-to-end verification of a correctly commanded I/O output. On the issuance of a discrete output to a relay, an unused relay point could be used to tie to a discrete I/O input. Ideally, the discrete input would take place following the completion of the commanded action.

4.2.4 TELEMETRY DATA STORAGE TRADE

A trade study was performed to determine the recommended method of implementing a telemetry buffer to temporarily store telemetry data prior to transferring the data to either the tape recorders or to the communications subsystem. The options were to provide a separate, redundant 4K 16-bit word buffer or to incorporate the additional storage requirement in main memory.

Functional requirements for the operation of a telemetry buffer are:

1. Housekeeping data is to be received from SEPS subsystems at 32 bps.
2. The computer formats the data and transfers it to the buffer at 32 bps.

3. When the buffer is full (every 2000 seconds), the buffer transfers data to the tape recorder at 32 Kbps, taking approximately 2 seconds.
4. Once per week, the tape recorder transfers data to the buffer at 1 Mbps until full.
5. The buffer then transfers the data to the communications subsystem at 1 Kbps.
6. Steps 4 and 5 are repeated until all the data is transmitted to the ground.
7. All data transfers are under control of the computer or ground command.
8. The buffer need not be random access (operation is first in-first out).

Using these assumptions, a preliminary design was performed for a separate buffer using low power off-the-shelf CMOS devices except for TTL line drivers. A non-redundant version has a volume of approximately 4000 cm^3, weighs 4.6 Kg and consumes approximately 5 watts of power including an assumed 65% power supply efficiency.

Table 4-5 summarizes the results of the trade. System reliability including the TM function in the CCS is higher with three separate TM buffers; however, the overall CCS reliability is still adequate with the 4K buffer in the fault tolerant memory. Five faults are tolerated with a 24K memory vs. two faults with a redundant external buffer. The trade is approximately even in power required since memory utilizes a low power switching mode when not addressed. Development cost favors the buffer in main memory. The 20K

Table 4-5. TM Buffer Trade Data

SYSTEM PARAMETER	20K F.T. MEMORY + SEPARATE 4K TM BUFFER	24K F.T. MEMORY
CCS Reliability	0.95650	0.94991
Redundancy	Tolerates 2 Faults	Tolerates 5 Faults
CCS Power (Average)	43.3 Watts	42.4 Watts
Dev. Costs*	5	<1
Recurring Costs*	5	2
Weight Delta	+14 Kg (+30 Lb)	Negligible
Interconnection Complexity	High	Very Low

*Relative costs on a scale of 1-10. Higher numbers represent higher costs.

of memory requires the integration costs of three slices (8K + 8K + 4K).of main storage; each is identical except the BSM's on the third page contain half the number of chips as those on the 8K pages. However, development and production of the separate triplex TM buffer is unique. To go from 20K to 24K no redesign is required. Recurring costs for a 24K memory are only the cost of fully populating an existing designed 8K page. Finally, a weight penalty of approximately 14 Kg is incurred with a separate memory. The weight of additional memory chips to go from 20K to 24K is negligible, less than the allowable tolerance on the weight of conformal coatings applied to slices or boards from computer to computer. Finally, the interconnections of three separate 4K buffers is more complex than that of the addition of 4K of storage to a proven 20K fault tolerant memory.

Considering the above, a 24K fault tolerant memory has been baselined, incorporating the 4K telemetry buffer in main memory.

4.2.5 CCS BASELINE DEFINITION

4.2.5.1 General

Figure 4-22 presents a block diagram of the SEPS CCS baseline. The main differences from the Reference 2 baseline are:

- The HTC was recommended as the baseline CCS computer. It has a 16-bit data flow CPU capable of executing 86 System 360 instructions.

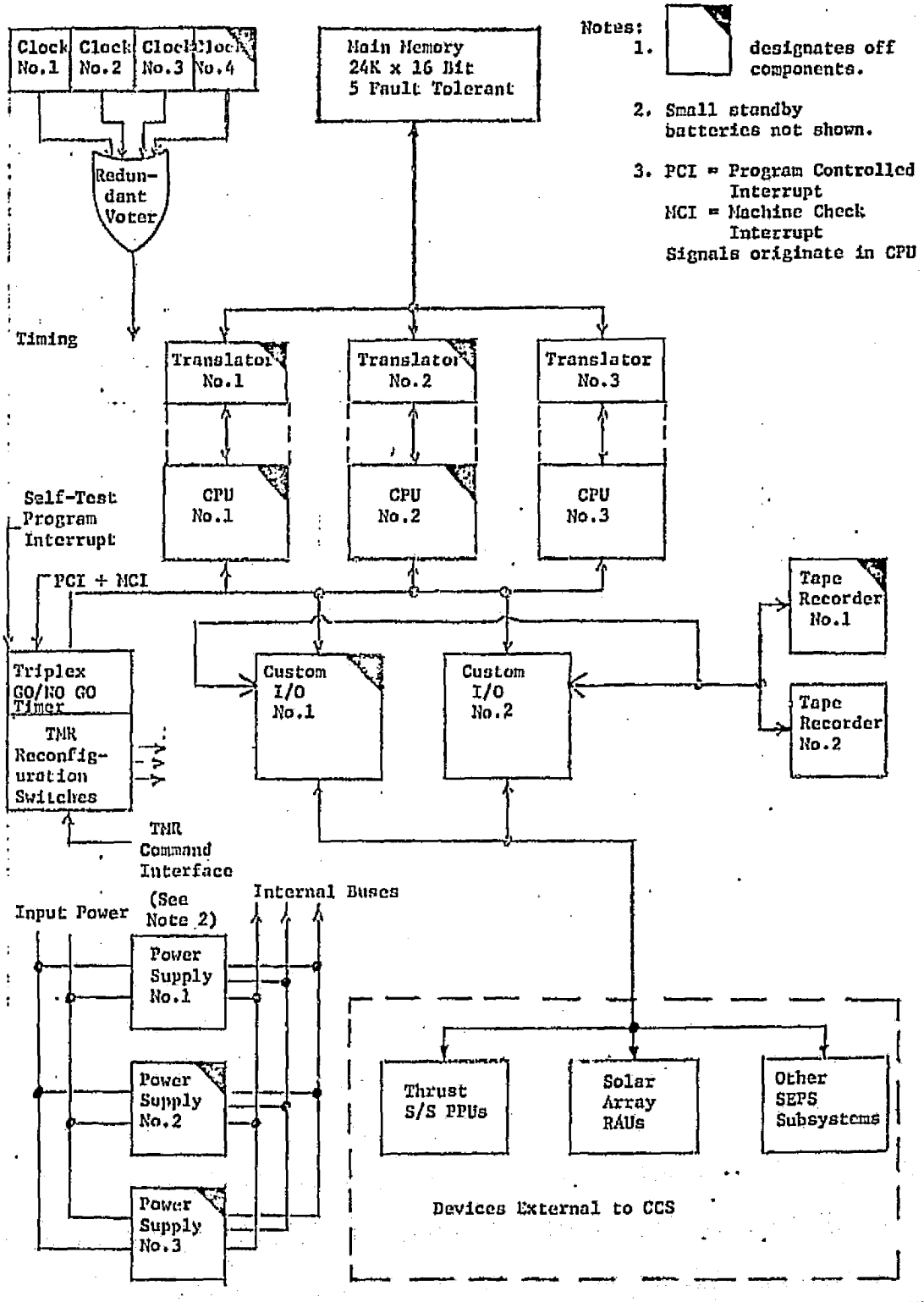


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Figure 4-22. SEPS Baseline CCS Block Diagram

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- o An increase in size of the 5 fault tolerant memory from 16K of 16-bits to 24K of 16-bits, which includes 4K telemetry buffer and approximately 50% contingency.
- o An increase of one translator and a philosophy which dedicates translators to CPU's.
- o The addition of two tape recorders.
- o A redesigned custom I/O which incorporates most of the subsystem RAU functions and from which miscellaneous vehicle sensors (pressure, bridge networks, etc.) and relays are excited.
- o Small standby batteries to power memory, clocks and reconfiguration switches in event of momentary loss of bus or regulated power supply.
- o Recommendation to not use high order language for software programming.

This computer configuration is similar to that proposed by IBM to MSFC for the Large Space Telescope (LST). Table 4-6 gives details of the HTC characteristics.

4.2.5.2 Computer/I/O Physical Characteristics

Packaging concepts for SEPS are as follows:

1. No cable harnesses are used for reliability improvement

Table 4-6. SUMC/HTC Characteristics

Type:	General-Purpose, Stored Program, Parallel
Organization:	Fixed Point, Binary, Integer
Storage:	Monolithic Random Access: 650 NS (N-MOS) Interface
Capacity:	65,536 bytes with density 8K x 16-bits
Storage Cycle Time:	650 NS
Addressable Unit:	8-bit byte
Internal Data Flow:	16-bit Parallel
Instruction Set:	86 Fixed Point Standard S/360 Instructions
Instruction Length:	16/32/48 bits
Data Word Length:	16/32/64 bits
Interrupt Facilities:	Single hardware with multilevel capability through hardware and software mechanization

Typical Execution Times:

Instructions:	16-Bit Data Flow CPU
Add (Register to Register)	2.0 μ S
Add (Register to Storage)	3.2 μ S
Multiply (32 x 32 Operand)	28.0 μ S
Average Processing Rate	250 KOPS

Features:

- S/360 Problem State Compatible
- Input/Output
  - Externally Initiated - Direct Memory Access, Buffered I/O
  - Program Initiated - Direct I/O, External Interrupts
- Storage Protect - Block, 512 Words
- Parity - Byte

C-2

and low cost. All interconnections are via multi-layer interconnection boards.

2. Pluggable assemblies are used for ease of in-process testing and repair.
3. Maximum use is made of LSI (consistent with technology) for minimum weight and increased reliability.
4. Multi-chip hybrid packaging of LSI logic is used to increase circuit density.

Modular Packaging Design Considerations

The SEPS packaging concept includes modular sub-assemblies using flexible printed wiring circuitry for electrical interconnections along with the multi-layer interconnection board (MIB). The sub-assemblies containing electrical components mounted on the MIBs are self-contained modules as illustrated in Figure 4-23. The unit assembly will be composed of the required modules electrically plugged into the backpanel and mechanically attached to the side rails of the structure as shown in Figure 4-24.

Page type and thickness vary and depend upon the style and type of electrical components used. Also, page thickness varies because of the number of interfacing lines between MIBs and backpanel necessary to make them self contained. The pages consist of two MIBs bonded to each side of an aluminum

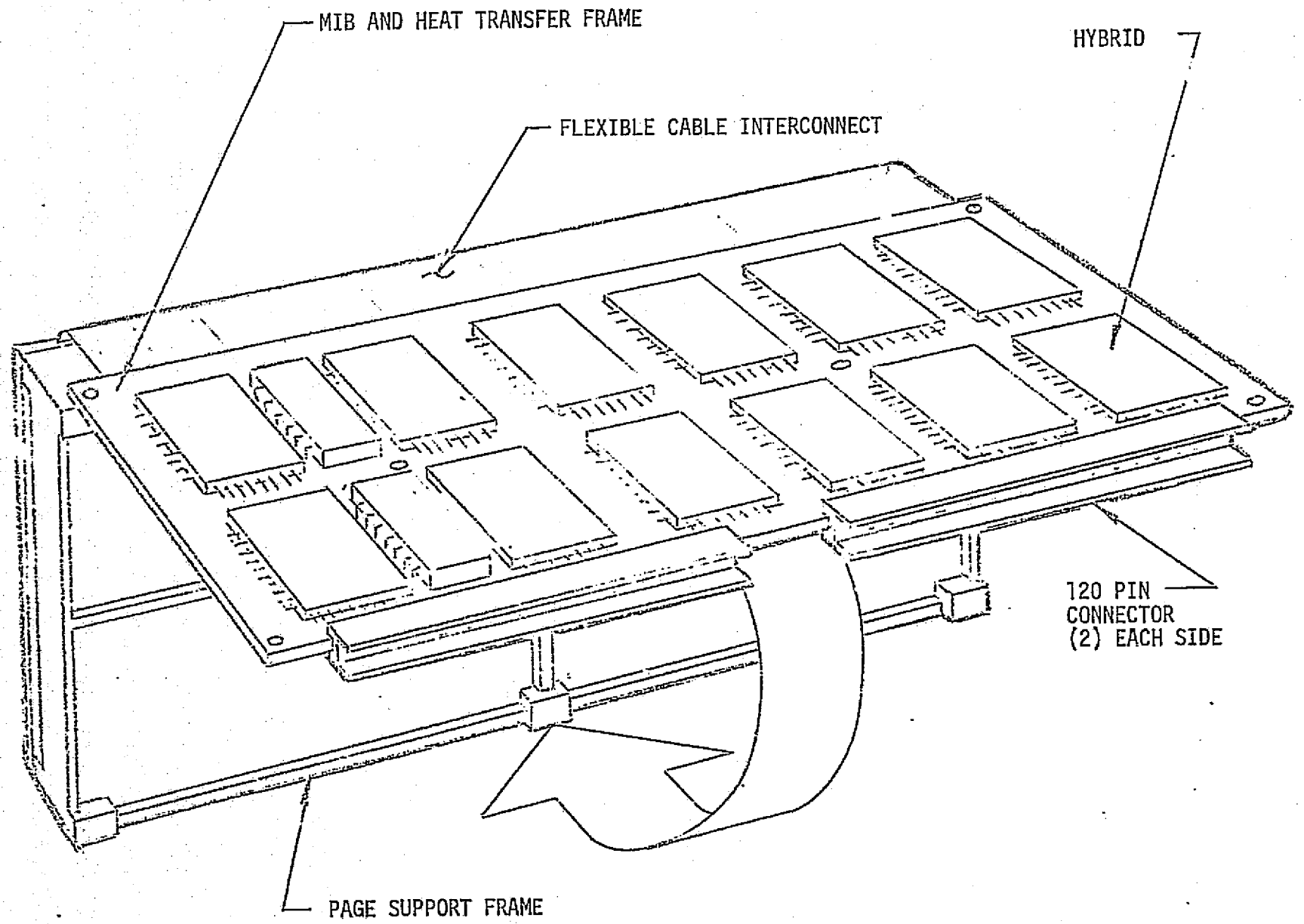

Figure 4-23. Electrical Component Sub-Assembly Packaging

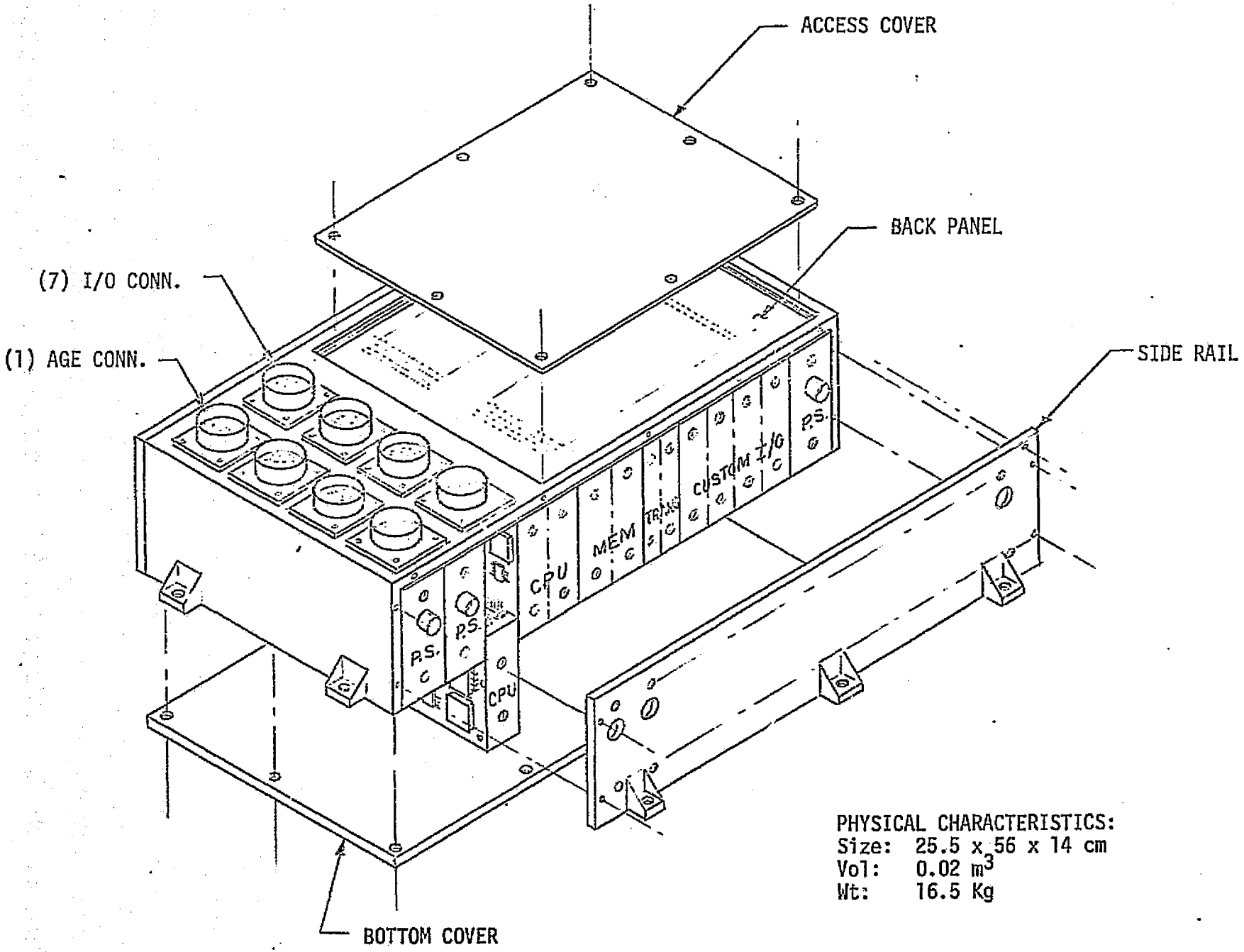

Figure 4-24. Computer/I/O Unit Assembly Packaging

heat transfer frame. Two 120 pin connectors are attached to the upper edge of the MIB to provide a pluggable interface with the motherboard/backpanel assembly. The page frame side surfaces are mechanically attached to the side rails which comprise the side of the unit assembly structure and also act as the heat transfer interface between the page, unit assembly and the heat transfer medium. The mounting feet on the end of the structure and the side rails are the heat transfer interface (bottom cover heat sink). The main frame of the unit structure is U-shaped and has mechanically attachable side rails and covers for ease of assembly and accessibility.

Special circuits are contained in modules and utilize hybrid technology. Each circuit is a mix of monolithic chips and thick film components. Special circuits are of various sizes with 1" x 1" being the most common. Logic chips are also packaged in hybrid submodules, typically 5 or 6 chips per container. Figure 4-25 illustrates the multi-chip packaging concept. Memory chips, because of a uniform and relatively small interconnection, are packaged more densely.

The hybrid power supply components are attached to a frame and make electrical interconnect with a printed wiring board using solder lands. The subassembly is pluggable to the backpanel and is attached to the side rails of the frame. External connectors are provided for prime power input.

External interface circuits are connected through high density circular connectors which have printed wiring board solder tails on the end of rear removable pins. These connectors interface directly with the motherboard and are fastened to the U-shaped main frame.

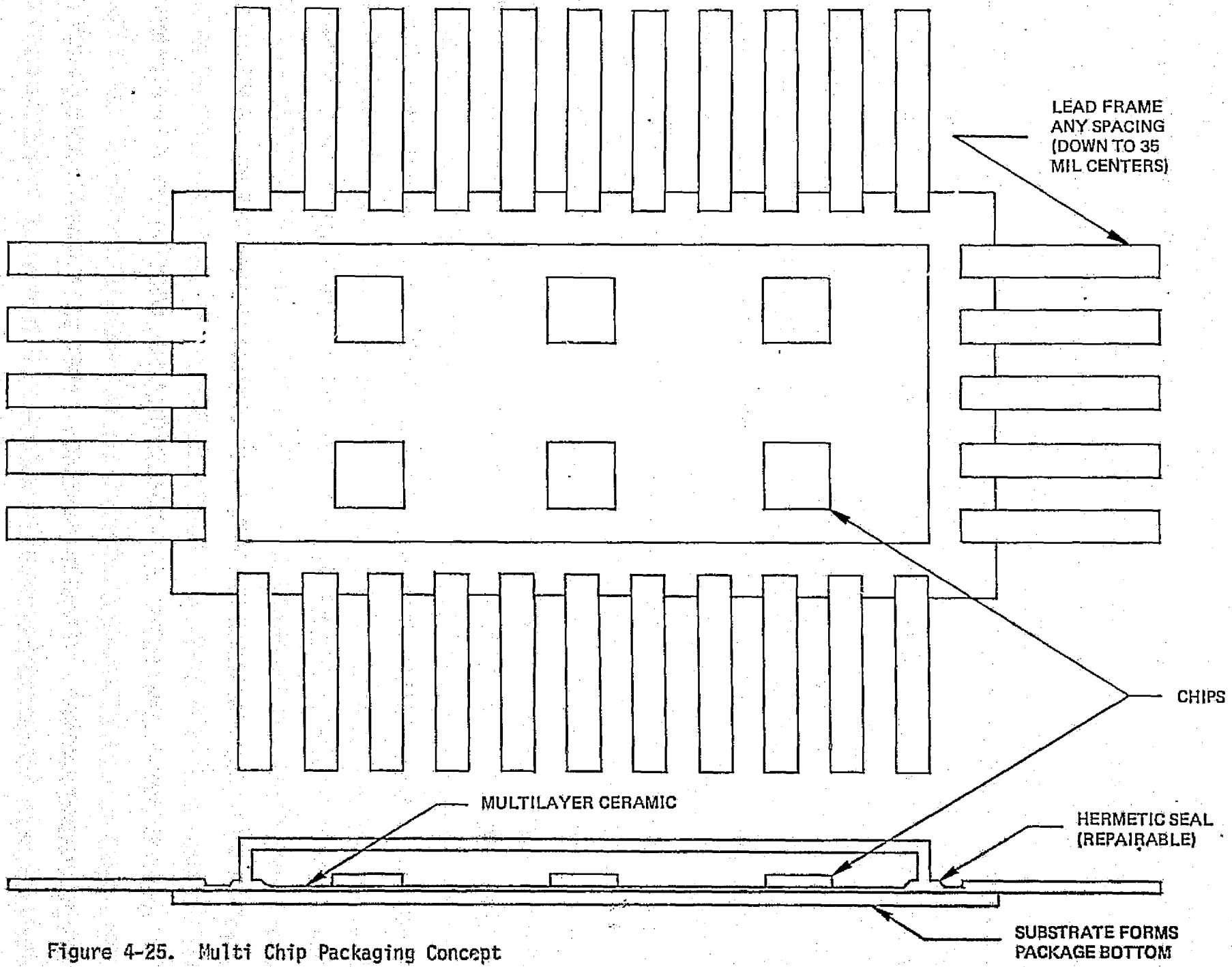

Figure 4-25. Multi Chip Packaging Concept

A summary of Computer/I/O packaging characteristics is presented below:

Size (L x W x H)	25.5x56x14 cm
Volume	0.02 m^3
Weight	16.5 Kg
Total No. of Pluggable Pages	11
No. Power Supplies	3

REDUNDANCY MANAGEMENT AND RELIABILITY ANALYSIS 5

5.1 GENERAL

Since the last study was performed (Reference 2) some basic groundrule changes occurred which had significant impacts on the CCS reliability and redundancy management. These were:

(1) CCS reliability goal was changed from 0.9703 to 0.9500 for a three-year unmaintained mission.

(2) Dual redundant tape recorders are a part of the CCS. Tape recorder reliability is 0.99981 for dual tape recorders for a three-year mission lifetime (Reference 11).

(3) CCS shall be capable of storing 4K of 16-bit words of telemetry data and periodically transmitting this data either to tape recorders or to the communications subsystem.

In order to accommodate these changes, a reliability and redundancy management analysis was performed. Major inputs to this analysis were the results of trade studies and analyses which were performed and are documented in other sections of this report. These are:

(1) Utilize a Hybrid Technology Computer (HTC) with a 16-bit data flow, NMOS memory technology, and bi-polar CPU logic design (Reference Sections 4.2.1 and 4.2.2).

(2) Incorporate the data acquisition function of data conversion, formatting, and code/decoding into the CCS with the exception of two subsystem interfaces: solar array and propulsion subsystems (Reference Section 4.2.3.2.1).

(3) Incorporate the 4K-word telemetry buffer into main memory (Reference Section 4.2.5).

(4) Memory size requirements, including contingency and the 4K-word telemetry data storage requirement, is 24K of 16-bit words (Reference Section 3.2.1).

For this study all CCS component failure rates were refined. A much better extimate of failure rates was possible with the current CCS configuration because they are predicated to a large extent on hardware that has been delivered. The HTC has been delivered to MSFC, the translator design is approximately 90% developed, and the fault tolerant memory breadboard is being fabricated. This permits a much more accurate prediction of failure rates and piece-part counts than was possible in the previous study. The failure rates assume high reliability parts procurement and fabrication programs and extensive component burn-in and screening.

5.2 COMPUTER

5.2.1 MAIN MEMORY

The organization, operation, and redundancy management techniques of the fault tolerant memory was not changed from that presented in the previous study. The memory size was increased to 24K of 16-bit words, however, and the switching circuitry between the memory and CPU/translator was simplified by changing the way spare bit planes are used. Now spare bit planes are switched as specific replacements for failed memory planes thus leaving uneffected all the other memory planes containing no errors. (For additional explanation see Section 4.2.2.2).

Early in the study an analysis was performed to relate memory reliability with memory size and with the number of memory faults to be accommodated. This was necessary input into the trade study concerning the location of the 4K word telemetry buffer (Reference Section 4.2.5). Figure 5-1 summarizes this data. For memory sizes greater than 16K, a five fault tolerant memory is required.

Because of the inherent nature of the fault tolerant memory design, the on/off failure rate ratio was assumed to be one, since all segments of memory are potentially required at any time. Coverage was assumed to be 0.99.

5.2.2 CPU/TRANSLATOR

Trade data was developed to assist in the performance of the trade study documented in Section 4.2.2.2 to determine the baseline SEPS CPU. Table 5-1 summarizes this data. Even though the reliability of the selected configuration was the lowest of the candidate concepts, it was adequate to meet the overall CCS reliability goal.

The CPU redundancy management scheme of having 3 CPUs with one operating and 2 spares was retained. Fault detection continues to be implemented by CPU self-tests and GO/NO-GO counters. A current study underway for MSFC indicates the addition of microcode storage parity checks will be necessary to achieve the assumed CPU coverage of 0.99. However, this is a small impact on the design. An on/off failure rate ratio of 4 was used.

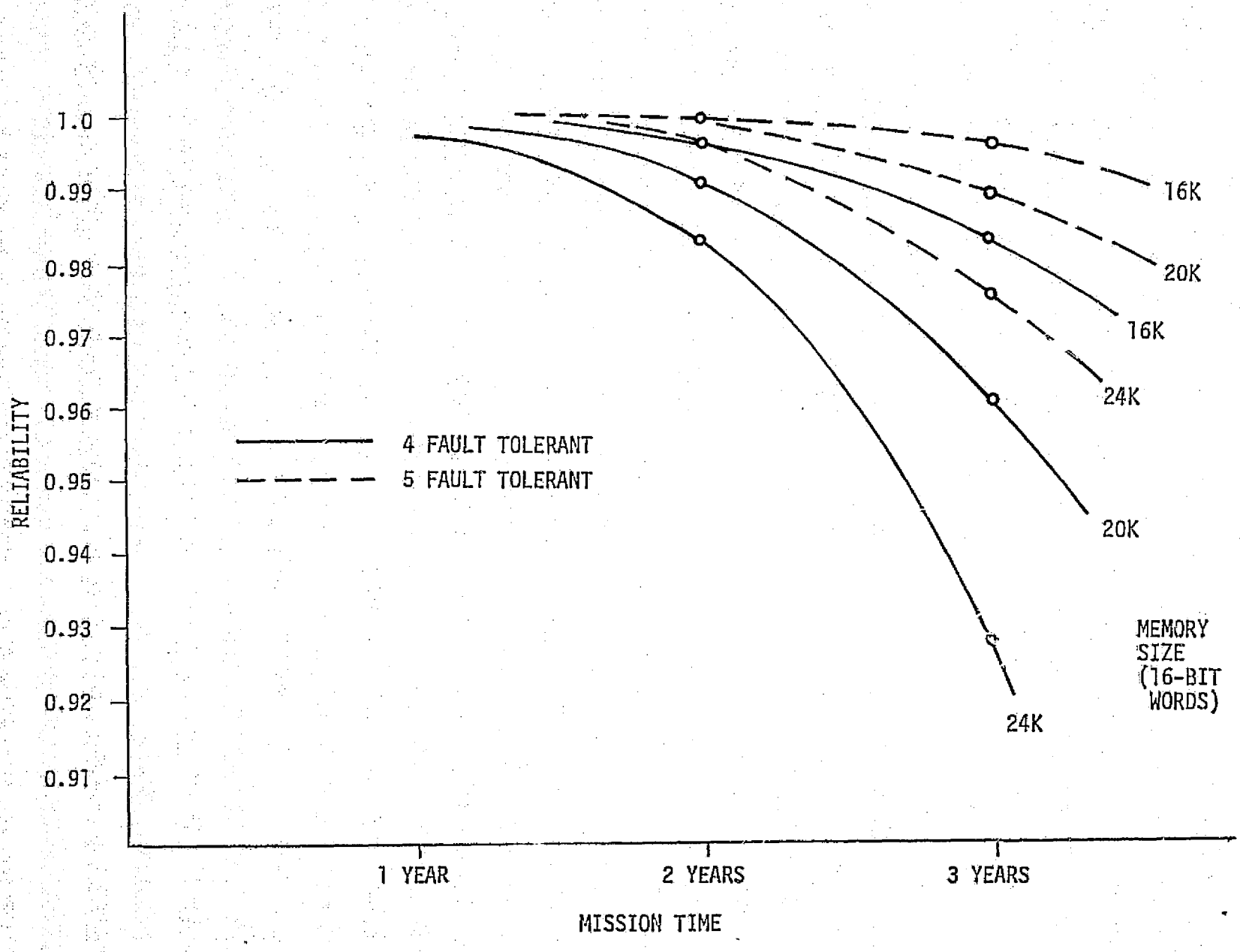

Figure 5-1. Memory Reliability vs SEPS Mission Time

Table 5-1. Summary CPU Trade Data

CPU Configuration	Instruction Set	Failures x 10^{-6} Hrs.	3 Year Reliability	Comment
8-Bit Data Flow TTL-LSI	TC-2 (47)	2.82	0.99914	Previous Baseline
8-Bit Data Flow TTL-LSI	S/360 (80)	4.20	0.99851	Candidate
8-Bit Data Flow N-MOS - LSI	S/360 (80)	2.59	0.99922	Candidate
16-Bit Data Flow TTL-LSI	S/360 (86)	5.56	0.99769	New Baseline

A change was made in the number of translators from that baselined in the previous study. It was determined that significant CPU/translator switching circuitry could be saved by having three translators, one dedicated to each CPU.

5.2.3 CLOCK

The clocks and associated oscillators are physically part of the power supplies. However, as discussed in paragraph 4.2.2.3, the clocks cannot be powered-down at any time because of the necessity to maintain memory cycling in failure recovery strategies. Therefore, the clocks are triple-modular-redundant (TMR) with one spare off as proposed in the previous study. Coverage and the on/off failure rate ratio were assumed to be 0.99 and 1, respectively.

5.2.4 POWER SUPPLY

Similar to the previous study, three hybrid power supplies are necessary to meet the reliability goal for SEPS and to achieve a balance of allocated reliability within the CCS. Only one supply is powered-on at a time. Detection and reconfiguration is achieved by measurement of over and undervoltage and overcurrent. Simple diode isolation of supply voltages probably can be achieved with adequate regulation. Coverage and on/off failure rate ratio were assumed to be 0.99 and 4, respectively.

5.2.5 RECONFIGURATION SWITCHING

The logical methods of reconfiguration presented in the previous study were re-examined and found to be adequate. However, packaging of these switches was not. Accordingly, this study treated the subject and allocated a conservative unreliability estimate to the many redundant switches which achieve the crosstrapping of functional elements (i.e., memory to 3 CPU's and 3 CPU's to 2 custom I/O's). The major factor in the design is the number of interconnections versus the number of gates required for switching. MSI flatpack technology yields the highest number of available leads/gate while LSI chip technology yields the greater number of gates/lead. A detailed design was not possible within the scope of this contract; therefore, only an approximation of a failure rate could be accomplished. The reconfiguration switches were assumed to be a combination of MSI flatpacks and LSI chips operating as TMR with a powered-off spare. Coverage and on/off failure rate ratio were assumed to be 0.99 and 1, respectively.

5.2.6 RECONFIGURATION CONTROL UNIT/SWITCH-OVER DETECTOR UNIT

The unit which detects failures (except in memory) and directs subsequent actions is the reconfiguration control unit/switch-over detector unit. It

contains the status registers for all spares, receives the various fault detection signals (CPU, I/O, Power Supply), and issues commands to the reconfiguration switches upon detection of a fault. Reconfiguration may be commanded from the ground via the custom I/O thus bypassing the CPU. Also contained in this unit is a GO/NO-GO window timer which must be reset during a preset time gate, or else a backup CPU or custom I/O will be switched in. Since this unit must be highly reliable and possess masking redundancy, a TMR/sparing technique is again proposed like the previous study. Coverage and on/off failure rate ratio were assumed to be 0.99 and 1, respectively.

5.2.7 TAPE RECORDER

A reliability of 0.99981 for the dual-redundant tape recorders (one operating and one powered-off) was groundruled for this study (Reference 11).

5.3 CUSTOM I/O

The custom I/O is primarily dual redundant with TMR logic for critical circuits such as the command interface logic and interrupt logic. One-half of the redundant I/O and the TMR logic is operating and the other one-half is powered-off. Error detection is provided by a BITE register, parity checks and feedback wrap tests. Fault detection will result in the generation of an interrupt to the CPU to automatically switch to the spare I/O section. Reference Section 4.2.3 for more detail on the redundant design aspects of the custom I/O. Coverage and on/off failure rate ratio were assumed to be 0.99 and 4, respectively.

5.4 TOTAL CCS

Figure 5-2 is a summary block diagram showing component failure rates, component redundancy levels and component reliability for a SEPS three-year,

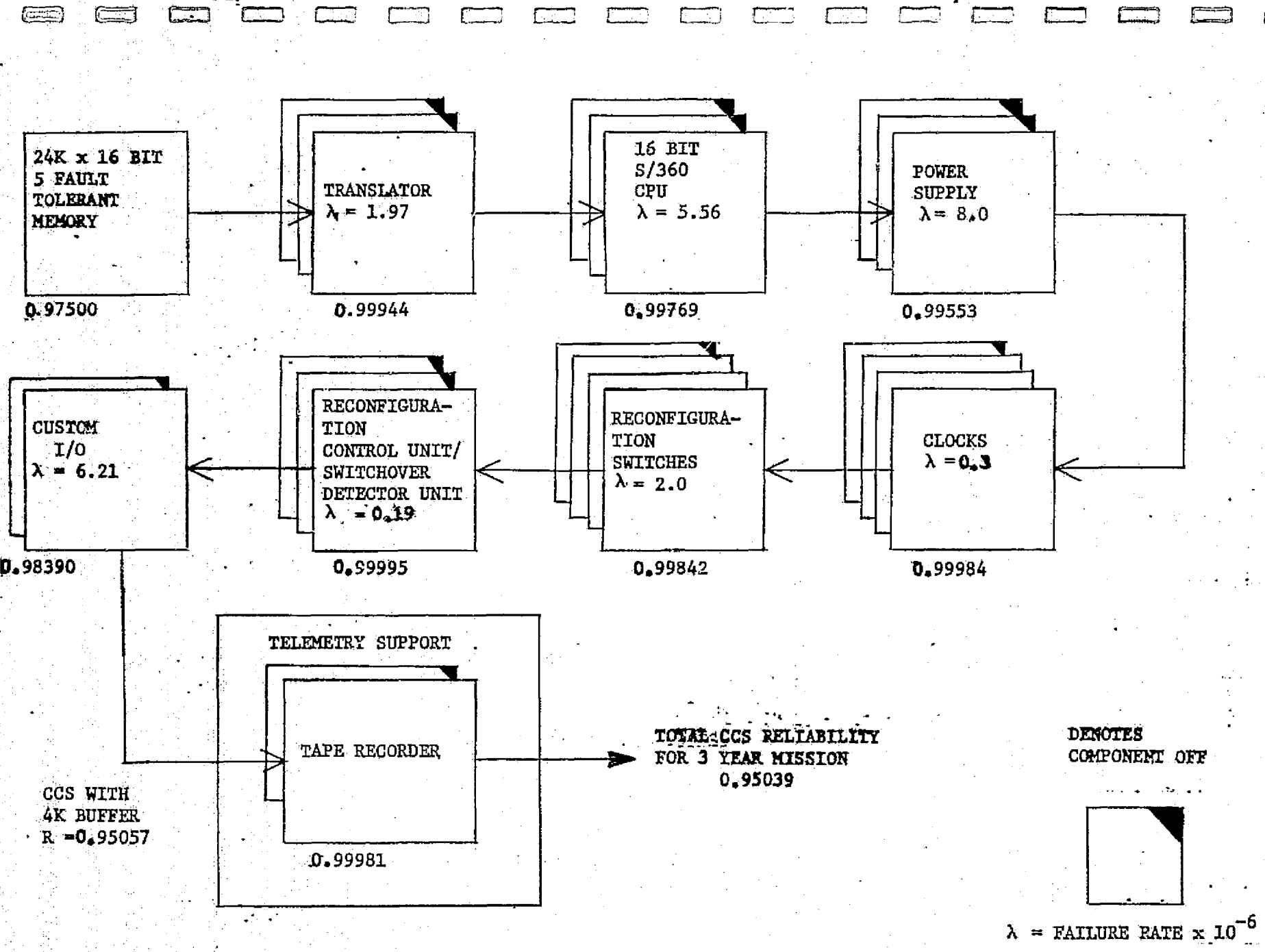

Figure 5-2. CCS Reliability Diagram

unmaintained mission. Total CCS reliability is calculated to be 0.95039, which exceeds the CCS reliability goal of 0.95000. Additionally, it should be noted that the above reliability estimate includes the unreliability contributed by equipment performing (1) telemetry formatting, storage and recording functions and (2) the bulk of data acquisition, formatting, and conditioning for the other SEPS subsystems.

Table 5-2 summarizes the CCS component redundancy characteristics.

Table 5-2. CCS Component Redundancy Characteristics

Component	Redundancy Characteristics
Main Memory	5 Fault Tolerant (4 spare bit planes)
Translator	1 Active, 2 Spares Off (Corrects 1 memory failure)
CPU	1 Active, 2 Spares Off
Power Supplies	1 Active, 2 Spares Off (With battery backup)
Clock	TMR + 1 Spare Off (Masking Redundancy)
Reconfiguration Switches	TMR + 1 Spare Off (Masking Redundancy)
Reconfiguration Control Unit	TMR (Masking Redundancy)
Custom I/O	1 Active, 1 Spare Off (Selected Circuits are TMR)
Tape Recorder	1 Active, 1 Spare Off

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5. IBM EMC Engineering Bulletin, Application of EMC Principles - Digital Computers, Chapter 9 - EMC Design Guide (EEB 3-2020 0027)

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NAS8-21176, DCN-1-7-40-79245, Martin Marietta Corporation, Denver Division, March 1968.

9. R. J. Mohr, "Coupling Between Open and Shielded Wire Lines Over a Ground Plane," IEEE Transactions on Electromagnetic Compatibility, Vol. EMC-9, pages 34-45, September 1967.

10. R. J. Mohr, "Interference Coupling - Attack It Early," Engineering Design News, dated 1 July 1969, pp. 33-41.

11. Memo, J. B. Weddell of Rockwell International to A. P. McKinley of IBM, Subject: "Command Computer/Data Handling Subsystem Interfaces," dated 7 August 1974.

12. SEPS Guidance and Navigation Autonomy Analysis, Contract NAS8-30271, dated 31 December 1974 (To be issued).

APPENDIX A

SEPS CCS DETAILED INTERFACE REQUIREMENTS

Appendix A - Signal List Definitions:

Source:	Where signal originates
Destination:	Destination of signal
Type:	Typically one of following: Discrete (DIS) Analog (ANA) Digital (DIG)
Class:	Typically one of the following: a. Critical Command (Cr Cmd) b. Noncritical Command (N Cmd) c. TM data measurement (TM) d. Control data measurement (Control)
No. of Wires:	The number of signal wires coming into I/O or exiting from I/O
Impedance:	The impedance that must be driven by the I/O circuits or the source impedance of signals to be measured by I/O
Voltage:	Nominal voltage levels (or range) of outputs and inputs.
Resolution:	Resolution of digital or analog input/output signals.
No. of Words:	Where a signal contains multiple words, this column indicates the quantity.
Sampling or Update Rate:	Self Explanatory.
GND/CCS Logic:	Indicates if onboard logic exists to initiate the command or if it is a ground command only. A "CCS" indication in this column does not preclude it also being initiated from the ground.

Guidance, Navigation and Control Signal Interface List (CCS Outputs)

Signal Name/Symbol	Source	Dest.	Type	Class	No. of Wires	Imped.	Voltage	Resolu-tion	No. of Words	Sampling or Update Rate	GND/CCS Logic
Gyro #1 Enable/Disable	CCS	Gyro	DIS	Cr Comd	One	TBD	28V	NA	NA	As Req'd	CCS
Gyro #2 Enable/Disable	"	"	"	"	"	"	"	"	"	"	"
Gyro #3 Enable/Disable	"	"	"	"	"	"	"	"	"	"	"
Sun Sensor #1 Enable/Disable	"	Sun Sensor	"	"	"	"	"	"	"	"	"
Sun Sensor #2 Enable/Disable	"	"	"	"	"	"	"	"	"	"	"
Sun Sensor #3 Enable/Disable	"	"	"	"	"	"	"	"	"	"	"
Star Tracker #1 Enable/Disable	"	Star Tracker	"	"	"	"	"	"	"	"	"
Star Tracker #2 Enable/Disable	"	"	"	"	"	"	"	"	"	"	"
ACS Elec Enable/Disable	"	ACS Elec	"	"	"	"	"	"	"	"	GND
ACS Mode Control	"	"	DIS (7)	"	Seven	"	"	"	"	"	CCS
Ion Thruster 1 Pitch Gimbal	"	"	DIG	"	TBD	"	TBD	0.35%	One	"	"
Ion Thruster 2 Pitch Gimbal	"	"	"	"	"	"	"	"	"	"	"
Ion Thruster 3 Pitch Gimbal	"	"	"	"	"	"	"	"	"	"	"
Ion Thruster 4 Pitch Gimbal	"	"	"	"	"	"	"	"	"	"	"
Ion Thruster 5 Pitch Gimbal	"	"	"	"	"	"	"	"	"	"	"
Ion Thruster 6 Pitch Gimbal	"	"	"	"	"	"	"	"	"	"	"
Ion Thruster 7 Pitch Gimbal	"	"	"	"	"	"	"	"	"	"	"
Ion Thruster 8 Pitch Gimbal	"	"	"	"	"	"	"	"	"	"	"
Ion Thruster 9 Pitch Gimbal	"	"	"	"	"	"	"	"	"	"	"
Ion Thruster 10 Pitch Gimbal	"	"	"	"	"	"	"	"	"	"	"
Ion Thruster 1 Yaw Gimbal	"	"	"	"	"	"	"	"	"	"	"
Ion Thruster 2 Yaw Gimbal	"	"	"	"	"	"	"	"	"	"	"
Ion Thruster 3 Yaw Gimbal	"	"	"	"	"	"	"	"	"	"	"
Ion Thruster 4 Yaw Gimbal	"	"	"	"	"	"	"	"	"	"	"
Ion Thruster 5 Yaw Gimbal	"	"	"	"	"	"	"	"	"	"	"
Ion Thruster 6 Yaw Gimbal	"	"	"	"	"	"	"	"	"	"	"
Ion Thruster 7 Yaw Gimbal	"	"	"	"	"	"	"	"	"	"	"
Ion Thruster 8 Yaw Gimbal	"	"	"	"	"	"	"	"	"	"	"
Ion Thruster 9 Yaw Gimbal	"	"	"	"	"	"	"	"	"	"	"
Ion Thruster 10 Yaw Gimbal	"	"	"	"	"	"	"	"	"	"	"

Signal Interface List

Signal Name/Symbol	Source	Dest.	Type	Class	No. of Wires	Imped.	Voltage	Resolution	No. of Words	Sampling or Update Rate	GND/CCS Logic
RCS Thruster 1 On/Off	CCS	RCS Thruster	DIS	Cr Comd	One	TBD	TBD	NA	NA	1/Sec	CCS
.	"	"	"	"	"	"	"	"	"	"	"
.	"	"	"	"	"	"	"	"	"	"	"
.	"	"	"	"	"	"	"	"	"	"	"
.	"	"	"	"	"	"	"	"	"	"	"
RCS Thruster 16 On/Off	"	"	"	"	"	"	"	"	"	"	"
*RCS Thruster 17 On/Off	"	"	"	"	"	"	"	"	"	"	"
.	"	"	"	"	"	"	"	"	"	"	"
.	"	"	"	"	"	"	"	"	"	"	"
.	"	"	"	"	"	"	"	"	"	"	"
.	"	"	"	"	"	"	"	"	"	"	"
*RCS Thruster 26 On/Off	"	"	"	"	"	"	"	"	"	"	"
RCS Thruster 1 Heater On/Off**	"	"	"	"	"	"	"	"	"	1/Min	"
.	"	"	"	"	"	"	"	"	"	"	"
.	"	"	"	"	"	"	"	"	"	"	"
.	"	"	"	"	"	"	"	"	"	"	"
.	"	"	"	"	"	"	"	"	"	"	"
RCS Thruster 16 Heater On/Off	"	"	"	"	"	"	"	"	"	"	"
*RCS Thruster 17 Heater On/Off	"	"	"	"	"	"	"	"	"	"	"
.	"	"	"	"	"	"	"	"	"	"	"
.	"	"	"	"	"	"	"	"	"	"	"
.	"	"	"	"	"	"	"	"	"	"	"
.	"	"	"	"	"	"	"	"	"	"	"
*RCS Thruster 26 Heater On/Off	"	"	"	"	"	"	"	"	"	"	"
RCS Hydrazine Isolation Valve 1 Open/Close	"	Valve	DIS	Cr Comd	One	"	"	"	"	1/10 Sec	"
RCS Hydrazine Isolation Valve 2 Open/Close	"	Valve	DIS	"	One	"	"	"	"	"	"
***RCS Krypton Isolation Valve 1 Open/Close	"	"	"	"	"	"	"	"	"	"	"
***RCS Krypton Isolation Valve 2 Open/Close	"	"	"	"	"	"	"	"	"	"	"
RCS Hydrazine Line 1 Heater On/Off	"	Heater	"	"	"	"	"	"	"	As Req'd	GND
*RCS Hydrazine Line 2 Heater On/Off	"	"	"	"	"	"	"	"	"	As Req'd	"

*Earth Orbital Missions Only
**Prior to firing RCS thrusters, temp is monitored for low threshold limit
***Planetary missions only; mission dependent

Signal-Interface List

Signal Name/Symbol	Source	Dest.	Type	Class	No. of Wires	Imped.	Voltage	Resolution	No. of Words	Sampling or Update Rate	GND/CCS Logic
*** RCS Krypton Line 1 Heater On/Off	CCS	Heater	DIS	Cr Comd	One	TBD	TBD	NA	NA	As Req'd	GND
*** RCS Krypton Line 2 Heater On/Off	"	"	"	"	"	"	"	"	"	"	"
-	CCS	***AGS	TO BE SUPPLIED								
-	CCS	*Laser Radar	" " "		ESTIMATE 15 DISCRETES						
-	CCS	*TV	" " "								
-	CCS	*Floodlights	" " "								
-	"	*Penlites	" " "								

TOTALS	DIG	DIS	ANALOG
Planetary	20	58	0
Earth Orbital	20	84	0

*Earth Orbital Missions only
***Planetary missions only; mission dependent

Guidance, Navigation and Control Signal Interface List (CCS Inputs)

Signal Name/Symbol	Source	Dest.	Type	Class	No. of Wires	Imped.	Voltage	Resolution	No. of Words	Sampling or Update Rate	GND/CCS Logic
Gyro #1 On/Off	Gyro	CCS	DIS	Control	One	560 Ω	5V	NA	NA	As Req'd	NA
Gyro #2 On/Off	"	"	"	"	"	"	"	"	"	"	"
Gyro #3 On/Off	"	"	"	"	"	"	"	"	"	"	"
Gyro #1 Rotor Speed	"	"	A	Control (RM)	Two	"	0-5V	1%	"	1/Min	"
Gyro #2 Rotor Speed	"	"	A	"	"	"	"	"	"	"	"
Gyro #3 Rotor Speed	"	"	A	"	"	"	"	"	"	"	"
Gyro #1 Temp	"	"	A	"	"	"	"	0.5%	"	"	"
Gyro #2 Temp	"	"	A	"	"	"	"	"	"	"	"
Gyro #3 Temp	"	"	A	"	"	"	"	"	"	"	"
Gyro #1 Rate Gimbal A	"	"	A	Control	"	"	TBD	"	"	1/Sec	"
Gyro #1 Rate Gimbal B	"	"	A	"	"	"	"	"	"	"	"
Gyro #2 Rate Gimbal A	"	"	A	"	"	"	"	"	"	"	"
Gyro #2 Rate Gimbal B	"	"	A	"	"	"	"	"	"	"	"
Gyro #3 Rate Gimbal A	"	"	A	"	"	"	"	"	"	"	"
Gyro #3 Rate Gimbal B	"	"	A	"	"	"	"	"	"	"	"
Sun Sensor 1 Output A	Sun Sensor	"	DIG	"	TBD	"	TBD	0.4%	"	"	"
Sun Sensor 1 Output B	"	"	"	"	"	"	"	"	"	"	"
Sun Sensor 2 Output A	"	"	"	"	"	"	"	"	"	"	"
Sun Sensor 2 Output B	"	"	"	"	"	"	"	"	"	"	"
Sun Sensor 3 Output A	"	"	"	"	"	"	"	"	"	"	"
Sun Sensor 3 Output B	"	"	"	"	"	"	"	"	"	"	"
Sun Sensor 1 On/Off	"	"	DIS	TM	One	"	5V	NA	"	1/Min	"
Sun Sensor 2 On/Off	"	"	"	"	"	"	"	"	"	"	"
Sun Sensor 3 On/Off	"	"	"	"	"	"	"	"	"	"	"
Sun Sensor 1 Temp	"	"	A	TM	Two	"	0-5V	1%	"	1/Min	"
Sun Sensor 2 Temp	"	"	A	"	"	"	"	"	"	"	"
Sun Sensor 3 Temp	"	"	A	"	"	"	"	"	"	"	"

(RM) = Redundancy Management

Signal Interface List

Signal Name/Symbol	Source	Dest.	Type	Class	No. of Wires	Imped.	Voltage	Resolution	No. of Words	Sampling or Update Rate	GND/CCS Logic
Star Tracker 1 Star Magnitude	Star Tracker	CCS	DIG	Control	TBD	560 Ω	TBD	12%	TBD	1/Sec	NA
Star Tracker 2 Star Magnitude	"	"	"	"	"	"	"	"	"	"	"
Star Tracker 1 Angle A	"	"	"	"	"	"	"	0.12%	"	"	"
Star Tracker 1 Angle B	"	"	"	"	"	"	"	"	"	"	"
Star Tracker 2 Angle A	"	"	"	"	"	"	"	"	"	"	"
Star Tracker 2 Angle B	"	"	"	"	"	"	"	"	"	"	"
Star Tracker 1 Temp	"	"	A	TM	Two	560 Ω	0-5V	1%	NA	1/Min	"
Star Tracker 2 Temp	"	"	A	"	"	"	"	"	"	"	"
Star Tracker 1 On/Off	"	"	DIS	Control	One	"	TBD	NA	"	1/Min	"
Star Tracker 2 On/Off	"	"	"	"	"	"	"	"	"	"	"
Ion Thruster 1 Pitch Gimbal	Actuator	"	A	Control	Two	TBD	"	0.35%	NA	1/10 Sec	"
.	"	"	.	"	"	"	"	"	"	"	"
.	"	"	.	"	"	"	"	"	"	"	"
.	"	"	.	"	"	"	"	"	"	"	"
.	"	"	.	"	"	"	"	"	"	"	"
Ion Thruster 10 Pitch Gimbal	"	"	A	"	"	"	"	"	"	"	"
Ion Thruster 1 Yaw Gimbal	"	"	A	"	"	"	"	"	"	"	"
.	"	"	.	"	"	"	"	"	"	"	"
.	"	"	.	"	"	"	"	"	"	"	"
.	"	"	.	"	"	"	"	"	"	"	"
.	"	"	.	"	"	"	"	"	"	"	"
Ion Thruster 10 Yaw Gimbal	"	"	A	"	"	"	"	"	"	"	"
RCS Thruster Valve 1 Status	Valve	"	DIS	"	One	TBD	"	NA	"	1/10 Sec	"
.	"	"	.	"	"	"	"	"	"	"	"
.	"	"	.	"	"	"	"	"	"	"	"
.	"	"	.	"	"	"	"	"	"	"	"
.	"	"	.	"	"	"	"	"	"	"	"
RCS Thruster Valve 16 Status	"	"	"	"	"	"	"	"	"	"	"
* RCS Thruster Valve 17 Status	"	"	"	"	"	"	"	"	"	"	"
* .	"	"	.	"	"	"	"	"	"	"	"
* .	"	"	.	"	"	"	"	"	"	"	"
* .	"	"	.	"	"	"	"	"	"	"	"
* .	"	"	.	"	"	"	"	"	"	"	"
* RCS Thruster Valve 26 Status	"	"	"	"	"	"	"	"	"	"	"

*Earth Orbital Missions only.

Signal Interface List

Signal Name/Symbol	Source	Dest.	Type	Class	No. of Wires	Imped.	Voltage	Resolution	No. of Words	Sampling or Update Rate	GND/CCS Logic
RCS Thruster 1 Temp	Thruster	CCS	A	Control	Two	TBD	TBD	3%	NA	1/Min	NA
.	"	"	.	"	"	"	"	"	"	"	"
.	"	"	.	"	"	"	"	"	"	"	"
.	"	"	.	"	"	"	"	"	"	"	"
RCS Thruster 16 Temp	"	"	"	"	"	"	"	"	"	"	"
* RCS Thruster 17 Temp	"	"	"	"	"	"	"	"	"	"	"
* .	"	"	.	"	"	"	"	"	"	"	"
* .	"	"	.	"	"	"	"	"	"	"	"
* .	"	"	.	"	"	"	"	"	"	"	"
* .	"	"	.	"	"	"	"	"	"	"	"
* RCS Thruster 26 Temp	"	"	"	"	"	"	"	"	"	"	"
RCS Thruster 1 Pressure	"	"	"	TM	"	"	"	5%	"	1/Sec	"
.	"	"	.	"	"	"	"	"	"	"	"
.	"	"	.	"	"	"	"	"	"	"	"
.	"	"	.	"	"	"	"	"	"	"	"
RCS Thruster 16 Pressure	"	"	"	"	"	"	"	"	"	"	"
* RCS Thruster 17 Pressure	"	"	"	"	"	"	"	"	"	"	"
* .	"	"	.	"	"	"	"	"	"	"	"
* .	"	"	.	"	"	"	"	"	"	"	"
* .	"	"	.	"	"	"	"	"	"	"	"
* .	"	"	.	"	"	"	"	"	"	"	"
* RCS Thruster 26 Pressure	"	"	"	"	"	"	"	"	"	"	"

*Earth Orbital Missions only

Signal Interface List

Signal Name/Symbol	Source	Dest.	Type	Class	No. of Wires	Imped.	Voltage	Resolution	No. of Words	Sampling or Update Rate	GND/CCS Logic
RCS Hydrazine Isolation Valve 1 Status	Valve	CCS	DIS	Control	One	TBD	TBD	NA	NA	1/10 Sec	NA
RCS Hydrazine Isolation Valve 2 Status	"	"	"	"	"	"	"	"	"	"	"
** RCS Krypton Isolation Valve 1 Status	"	"	"	"	"	"	"	"	"	"	"
** RCS Krypton Isolation Valve 2 Status	"	"	"	"	"	"	"	"	"	"	"
RCS Hydrazine Tank 1 Press	Tank	"	A	TM	Two	560 Ω	0-5V	5%	"	1/Sec	"
* RCS Hydrazine Tank 2 Press	"	"	A	"	"	"	"	"	"	"	"
RCS Hydrazine Tank 1 Temp	"	"	A	"	"	"	"	0.6%	"	1/Min	"
* RCS Hydrazine Tank 2 Temp	"	"	A	"	"	"	"	"	"	"	"
RCS Hydrazine Manifold Press	Manifold	"	A(4)	"	"	"	"	5%	"	1/Sec	"
** RCS Krypton Tank Press	Tank	"	A	"	"	"	"	"	"	"	"
** RCS Krypton Tank Temp	"	"	A	"	"	"	"	0.6%	"	1/Min	"
** RCS Krypton Manifold Press	Manifold	"	A(2)	"	"	"	"	5%	"	1/Sec	"
RCS Hydrazine Line 1 Temp	Line	"	A	"	"	"	"	1%	"	1/Min	"
* RCS Hydrazine Line 2 Temp	"	"	A	"	"	"	"	"	"	"	"
** RCS Krypton Line 1 Temp	"	"	A	"	"	"	"	"	"	"	"
** RCS Krypton Line 2 Temp	"	"	A	"	"	"	"	"	"	"	"
-	**AGS	"	TO BE SUPPLIED								
-	*Laser Radar	"	" " "								
-	*TV	"	" " "								
-	*Flood-lights	"	" " "								
-	*Penlites	"	" " "								

ESTIMATE 14 DIS
12 ANALOG

TOTALS	DIG	DIS	ANALOG
Planetary	12	32	86
Earth Orbital	12	46	107

*Earth Orbital Missions only
**Planetary missions only; mission dependent

Propulsion Subsystem Signal Interface List **(CCS Outputs)

	Signal Name/Symbol	Source	Dest.	Type	Class	No. of Wires	Imped.	Voltage	Resolution	No. of Words	Sampling or Update Rate	GND/CCS Logic
*	Power Processor #1 Control/Meas	CCS	Pwr Cond	DIG	Cr Cond	8	****	****	***	*****	1/Sec	CCS
*	Power Processor #2 Control/Meas	"	"	"	"	"	"	"	"	"	"	"
*	Power Processor #3 Control/Meas	"	"	"	"	"	"	"	"	"	"	"
*	Power Processor #4 Control/Meas	"	"	"	"	"	"	"	"	"	"	"
*	Power Processor #5 Control/Meas	"	"	"	"	"	"	"	"	"	"	"
*	Power Processor #6 Control/Meas	"	"	"	"	"	"	"	"	"	"	"
*	Power Processor #7 Control/Meas	"	"	"	"	"	"	"	"	"	"	"
*	Power Processor #8 Control/Meas	"	"	"	"	"	"	"	"	"	"	"
	PC/Thruster Sw A1	"	SW Matrix	DIS	"	One	"	28V	NA	NA	TBD	"
	PC/Thruster Sw A2	"	"	"	"	"	"	"	"	"	"	"
	PC/Thruster Sw B1	"	"	"	"	"	"	"	"	"	"	"
	PC/Thruster Sw B2	"	"	"	"	"	"	"	"	"	"	"
	PC/Thruster Sw C1	"	"	"	"	"	"	"	"	"	"	"
	PC/Thruster Sw C2	"	"	"	"	"	"	"	"	"	"	"
	PC/Thruster Sw D1	"	"	"	"	"	"	"	"	"	"	"
	PC/Thruster Sw D2	"	"	"	"	"	"	"	"	"	"	"
	PC/Thruster Sw E1	"	"	"	"	"	"	"	"	"	"	"
	PC/Thruster Sw E2	"	"	"	"	"	"	"	"	"	"	"
	PC/Thruster Sw F1	"	"	"	"	"	"	"	"	"	"	"
	PC/Thruster Sw F2	"	"	"	"	"	"	"	"	"	"	"
	PC/Thruster Sw G1	"	"	"	"	"	"	"	"	"	"	"
	PC/Thruster Sw G2	"	"	"	"	"	"	"	"	"	"	"
	PC/Thruster Sw H1	"	"	"	"	"	"	"	"	"	"	"
	PC/Thruster Sw H2	"	"	"	"	"	"	"	"	"	"	"

*These signals include both commands and measurements. One each, twisted pair for clock, frame, and data in/out.
**Assumes 10 thrusters, 8 power conditioners, 2 Hg tanks.
***CCS → PPU 7 bits (message data field bits 2-8)
PPU → CCS 6 bits (data response field bits 19-24)
****Open collector TTL line driver
*****24-bit word

Signal Interface List

Signal Name/Symbol	Source	Dest.	Type	Class	No. of Wires	Imped.	Voltage	Resolution	No. of Words	Sampling or Update Rate	GND/CCS Logic
Hg Tank Valve #1 Open	CCS	Valve Cont Module	DIS	Cr Comd	One	TBD	28V	NA	NA	2/Day	GND
Hg Tank Valve #1 Close	"	"	"	"	"	"	"	"	"	"	"
Hg Tank Valve #2 Open	"	"	"	"	"	"	"	"	"	"	"
Hg Tank Valve #2 Close	"	"	"	"	"	"	"	"	"	"	"
Thruster #1 Hg Valve Open	"	"	"	"	"	"	"	"	"	"	"
Thruster #1 Hg Valve Close	"	"	"	"	"	"	"	"	"	"	"
Thruster #2 Hg Valve Open	"	"	"	"	"	"	"	"	"	"	"
Thruster #2 Hg Valve Close	"	"	"	"	"	"	"	"	"	"	"
Thruster #3 Hg Valve Open	"	"	"	"	"	"	"	"	"	"	"
Thruster #3 Hg Valve Close	"	"	"	"	"	"	"	"	"	"	"
Thruster #4 Hg Valve Open	"	"	"	"	"	"	"	"	"	"	"
Thruster #4 Hg Valve Close	"	"	"	"	"	"	"	"	"	"	"
Thruster #5 Hg Valve Open	"	"	"	"	"	"	"	"	"	"	"
Thruster #5 Hg Valve Close	"	"	"	"	"	"	"	"	"	"	"
Thruster #6 Hg Valve Open	"	"	"	"	"	"	"	"	"	"	"
Thruster #6 Hg Valve Close	"	"	"	"	"	"	"	"	"	"	"
Thruster #7 Hg Valve Open	"	"	"	"	"	"	"	"	"	"	"
Thruster #7 Hg Valve Close	"	"	"	"	"	"	"	"	"	"	"
Thruster #8 Hg Valve Open	"	"	"	"	"	"	"	"	"	"	"
Thruster #8 Hg Valve Close	"	"	"	"	"	"	"	"	"	"	"
Thruster #9 Hg Valve Open	"	"	"	"	"	"	"	"	"	"	"
Thruster #9 Hg Valve Close	"	"	"	"	"	"	"	"	"	"	"
Thruster #10 Hg Valve Open	"	"	"	"	"	"	"	"	"	"	"
Thruster #10 Hg Valve Close	"	"	"	"	"	"	"	"	"	"	"

Signal Interface List

Signal Name/Symbol	Source	Dest.	Type	Class	No. of Wires	Imped.	Voltage	Resolu-tion	No. of Words	Sampling or Update Rate	GND/CCS Logic
Hg Feedline Heater #1 On/Off	CCS	Heater	DIS	Cr Comd	One	TBD	28V	NA	NA	2/Day	GND
Hg Feedline Heater #2 On/Off	"	"	"	"	"	"	"	"	"	"	"
Thruster Feedline Heater #1 On/Off	"	"	"	"	"	"	"	"	"	"	"
Thruster Feedline Heater #2 On/Off	"	"	"	"	"	"	"	"	"	"	"
Thruster Feedline Heater #3 On/Off	"	"	"	"	"	"	"	"	"	"	"
Thruster Feedline Heater #4 On/Off	"	"	"	"	"	"	"	"	"	"	"
Thruster Feedline Heater #5 On/Off	"	"	"	"	"	"	"	"	"	"	"
Thruster Feedline Heater #6 On/Off	"	"	"	"	"	"	"	"	"	"	"
Thruster Feedline Heater #7 On/Off	"	"	"	"	"	"	"	"	"	"	"
Thruster Feedline Heater #8 On/Off	"	"	"	"	"	"	"	"	"	"	"
Thruster Feedline Heater #9 On/Off	"	"	"	"	"	"	"	"	"	"	"
Thruster Feedline Heater #10 On/Off	"	"	"	"	"	"	"	"	"	"	"
TOTAL				DIG	DIS	ANALOG					
				8	52	0					

Propulsion Subsystem Signal Interface List (CCS Inputs)

Signal Name/Symbol	Source	Dest.	Type	Class	No. of Wires	Imped.	Voltage	Resolution	No. of Words	Sampling or Update Rate	GND/CCS Logic
Inputs from Power Processors have been accounted for in output list.											
Spare PPU Sw Position	SW Matrix	CCS	DIS (10)	Control	One	TBD	28V	NA	NA	TBD	NA
Spare Thruster #1 Sw Pos	"	"	DIS (9)	"	"	"	"	"	"	"	"
Spare Thruster #2 Sw Pos	"	"	DIS (9)	"	"	"	"	"	"	"	"
Hg Tank #1 Temp	Hg Tank	"	A	TM	Two	560 Ω	0-5V	1%	"	1/8 Min	"
Hg Tank #2 Temp	"	"	"	"	"	"	"	"	"	"	"
Hg Tank #1 Press	"	"	"	"	"	"	"	"	"	"	"
Hg Tank #2 Press	"	"	"	"	"	"	"	"	"	"	"
Hg Feedline #1 Temp	Lines	"	"	"	"	"	"	"	"	1/Hour	"
Hg Feedline #2 Temp	"	"	"	"	"	"	"	"	"	"	"
Hg Tank Valve #1 Open/Close	Valve Control Module	"	DIS	"	One	TBD	5V	NA	"	2/Day	"
Hg Tank Valve #2 Open/Close	"	"	"	"	"	"	"	"	"	"	"

Signal Interface List

Signal Name/Symbol	Source	Dest.	Type	Class	No. of Wires	Imped.	Voltage	Resolution	No. of Words	Sampling or Update Rate	GND/CCS Logic
Thruster #1 Hg Valve Open/Close	Valve	CCS	DIS	TM	One	TBD	5V	NA	NA	2/Day	NA
Thruster #2 Hg Valve Open/Close	"	"	"	"	"	"	"	"	"	"	"
Thruster #3 Hg Valve Open/Close	"	"	"	"	"	"	"	"	"	"	"
Thruster #4 Hg Valve Open/Close	"	"	"	"	"	"	"	"	"	"	"
Thruster #5 Hg Valve Open/Close	"	"	"	"	"	"	"	"	"	"	"
Thruster #6 Hg Valve Open/Close	"	"	"	"	"	"	"	"	"	"	"
Thruster #7 Hg Valve Open/Close	"	"	"	"	"	"	"	"	"	"	"
Thruster #8 Hg Valve Open/Close	"	"	"	"	"	"	"	"	"	"	"
Thruster #9 Hg Valve Open/Close	"	"	"	"	"	"	"	"	"	"	"
Thruster #10 Hg Valve Open/Close	"	"	"	"	"	"	"	"	"	"	"
Thruster #1 Feedline Temp	Line	"	A	"	Two	560 Ω	0-5V	1%	"	1/Hour	"
Thruster #2 Feedline Temp	"	"	"	"	"	"	"	"	"	"	"
Thruster #3 Feedline Temp	"	"	"	"	"	"	"	"	"	"	"
Thruster #4 Feedline Temp	"	"	"	"	"	"	"	"	"	"	"
Thruster #5 Feedline Temp	"	"	"	"	"	"	"	"	"	"	"
Thruster #6 Feedline Temp	"	"	"	"	"	"	"	"	"	"	"
Thruster #7 Feedline Temp	"	"	"	"	"	"	"	"	"	"	"
Thruster #8 Feedline Temp	"	"	"	"	"	"	"	"	"	"	"
Thruster #9 Feedline Temp	"	"	"	"	"	"	"	"	"	"	"
Thruster #10 Feedline Temp	"	"	"	"	"	"	"	"	"	"	"

TOTAL	DIG	DIS	ANALOG
	0	40	16

Communications Subsystem Signal Interface List (CCS Outputs)(1)

Signal Name/Symbol	Source	Dest.	Type	Class	No. of Wires	Imped.	Voltage	Resolution	No. of Words	Sampling or Update Rate	GND/CCS Logic
LGA Switch Reverse	CCS	Switch	DIS	Cr Comd	One	TBD	28V	NA	NA	<1/64 Min	CCS
(2) HGA Switch On/Off	"	"	DIS	"	"	"	"	"	"	Once	GND
(2) S-Band TWTA 1 On/Off	"	Control Logic Box	"	"	"	"	"	"	"	<1/32 Min	CCS
(2) S-Band TWTA 2 On/Off	"	"	"	"	"	"	"	"	"	"	"
(2) X-Band TWTA 1 On/Off	"	"	"	"	"	"	"	"	"	"	"
(2) X-Band TWTA 2 On/Off	"	"	"	"	"	"	"	"	"	"	"
S-Band Exciter 1 On/Off	"	"	"	"	"	"	"	"	"	<1/64 Min	"
S-Band Exciter 2 On/Off	"	"	"	"	"	"	"	"	"	"	"
Receiver 1 On/Off	"	"	"	"	"	"	"	"	"	<1/32 Min	"
Receiver 2 On/Off	"	"	"	"	"	"	"	"	"	"	"
Ranging On/Off	"	Receiver	"	"	"	"	"	"	"	1/6 Hour	GND
TMU 1 On/Off	"	TMU	"	"	"	"	"	"	"	TBD	CCS
TMU 2 On/Off	"	"	"	"	"	"	"	"	"	"	"
TMU 1 Channel Select	"	"	DIG	N Comd	TBD	"	TBD	2 Bits	TBD	<1/Day	CCS
TMU 2 Channel Select	"	"	"	"	"	"	"	"	"	"	"
TMU 1 Mod Angle	"	"	"	"	"	"	"	7 Bits	"	"	GND
TMU 2 Mod Angle	"	"	"	"	"	"	"	"	"	"	"
(3) TMU 1 Engr Data Rate	"	"	"	"	"	"	"	3 Bits	"	<1/32 Min	"
(3) TMU 2 Engr Data Rate	"	"	"	"	"	"	"	"	"	"	"
(3) TMU 1 Science Data Rate	"	"	"	"	"	"	"	12 Bits	"	"	"
(3) TMU 2 Science Data Rate	"	"	"	"	"	"	"	"	"	"	"
(2) X-Band Iso Sw Reverse	"	Switch	DIS	"	"	"	28V	NA	NA	<1/64 Min	CCS

(1) HGA gimbal commands/measurements are shown in structures and mechanisms
(2) Planetary missions only
(3) Attached science payload only; planetary missions only

Signal Interface List

Signal Name/Symbol	Source	Dest.	Type	Class	No. of Wires	Imped.	Voltage	Resolution	No. of Words	Sampling or Update Rate	GND/CCS Logic
(4) TV FM Xmitter Select	CCS	Xmitter	DIS		One	TBD	28V	NA	NA	TBD	CCS
(4) TV FM Xmitter 1 On/Off	"	"	"		"	"	"	"	"	"	"
(4) TV FM Xmitter 2 On/Off	"	"	"		"	"	"	"	"	"	"
(4) TV Mod Exciter 1 On/Off	"	Exciter	"		"	"	"	"	"	"	"
(4) TV Mod Exciter 2 On/Off	"	"	"		"	"	"	"	"	"	"

TOTAL	DIG	DIS	ANALOG
Planetary	8	14	0
Earth Orbital	4	13	0

(4) Earth Orbital missions only

Communications Subsystem Signal Interface List (CCS Inputs)

Signal Name/Symbol	Source	Dest.	Type	Class	No. of Wires	Imped.	Voltage	Resolution	No. of Words	Sampling or Update Rate	GND/CCS Logic
Command/Configuration Verify		CCS	DIG	TM	TBD	TBD	TBD	8 Bits	NA	<1/64 Min	NA
TMU 1 Osc Temp	TMU.	"	A	Control	Two	"	"	0.1%	"	"	"
TMU 2 Osc Temp	"	"	A	"	"	"	"	"	"	"	"
TMU 1 Subcarrier 1 Level	"	"	A	TM	"	"	"	1%	"	"	"
TMU 2 Subcarrier 1 Level	"	"	A	"	"	"	"	"	"	"	"
TMU 1 Subcarrier 2 Level	"	"	A	"	"	"	"	"	"	"	"
TMU 2 Subcarrier 2 Level	"	"	A	"	"	"	"	"	"	"	"
S-Band Exciter #1 Current	Exciter	"	A	Control	"	"	"	2%	"	"	"
S-Band Exciter #2 Current	"	"	A	"	"	"	"	"	"	"	"
S-Band Exciter #1 Output Level	"	"	A	"	"	"	"	"	"	"	"
S-Band Exciter #2 Output Level	"	"	A	"	"	"	"	"	"	"	"
* S-Band TWTA 1 Current	TWTA	"	A	"	"	"	"	"	"	<1/32 Min	"
* S-Band TWTA 2 Current	"	"	A	"	"	"	"	"	"	"	"
* S-Band TWTA 1 Temp	"	"	A	"	"	"	"	"	"	<1/64 Min	"
* S-Band TWTA 2 Temp	"	"	A	"	"	"	"	"	"	"	"
* S-Band TWTA 1 Output Level	"	"	A	"	"	"	"	"	"	<1/32 Min	"
* S-Band TWTA 2 Output Level	"	"	A	"	"	"	"	"	"	"	"
* X-Band TWTA 1 Current	"	"	A	"	"	"	"	"	"	"	"
* X-Band TWTA 2 Current	"	"	A	"	"	"	"	"	"	"	"
* X-Band TWTA 1 Temp	"	"	A	"	"	"	"	"	"	<1/64 Min	"
* X-Band TWTA 2 Temp	"	"	A	"	"	"	"	"	"	"	"
* X-Band TWTA 1 Output Level	"	"	A	"	"	"	"	"	"	<1/32 Min	"
* X-Band TWTA 2 Output Level	"	"	A	"	"	"	"	"	"	"	"
* X-Band Oscillator Temp	OSC	"	A	TM	"	"	"	"	"	TBD	"

*Planetary missions only

Signal Interface List

Signal Name/Symbol	Source	Dest.	Type	Class	No. of Wires	Imped.	Voltage	Resolution	No. of Words	Sampling or Update Rate	GND/CCS Logic
Receiver 1 Current	Receiver	CCS	A	Control	Two	TBD	TBD	3%	NA	<1/32 Min	NA
Receiver 2 Current	"	"	A	"	"	"	"	"	"	"	"
Receiver 1 Temp	"	"	A	"	"	"	"	"	"	<1/64 Min	"
Receiver 2 Temp	"	"	A	"	"	"	"	"	"	"	"
Receiver 1 AGC Level	"	"	A	"	"	"	"	1%	"	<1/32 Min	"
Receiver 2 AGC Level	"	"	A	"	"	"	"	"	"	"	"
Receiver 1 Static Phase Error	"	"	A	TM	"	"	"	3%	"	"	"
Receiver 2 Static Phase Error	"	"	A	"	"	"	"	"	"	"	"
** TV FM Exciter 1 Current	Exciter	"	A	Control	"	"	"	"	"	<1/64 Min	"
** TV FM Exciter 2 Current	"	"	A	"	"	"	"	"	"	"	"
** TV FM Exciter 1 Output Level	"	"	A	"	"	"	"	"	"	"	"
** TV FM Exciter 2 Output Level	"	"	A	"	"	"	"	"	"	"	"
** TV FM Xmitter 1 Current	Xmitter	"	A	"	"	"	"	"	"	<1/32 Min	"
** TM FM Xmitter 2 Current	"	"	A	"	"	"	"	"	"	"	"
** TV FM Xmitter 1 Temp	"	"	A	"	"	"	"	"	"	<1/64 Min	"
** TV FM Xmitter 2 Temp	"	"	A	"	"	"	"	"	"	"	"
** TV FM Xmitter 1 Output Level	"	"	A	"	"	"	"	"	"	<1/32 Min	"
** TV FM Xmitter 2 Output Level	"	"	A	"	"	"	"	"	"	"	"
Command Decoder A Output	Decoder	"	DIG	"	TBD	"	"	NA	***	As Req'd	"
Command Decoder B Output	"	"	DIG	"	"	"	"	"	***	"	"

TOTAL	DIG	DIS	ANALOG
Planetary	3	0	31
Earth Orbital	3	0	28

**Earth Orbital missions only
***Number of command words varies with the particular command

CCS Signal Interface List (Output)*

Signal Name/Symbol	Source	Dest.	Type	Class	No. of Wires	Imped.	Voltage	Resolu-tion	No. of Words	Sampling or Update Rate	GND/CCS Logic
Attitude Error Command											
±Pitch	CCS	TM Only	DIG	N Comd (TM only)	NA	NA	NA	0.35%	One	1/Min	CCS
±Roll	"	"	"	"	"	"	"	"	"	"	"
±Yaw	"	"	"	"	"	"	"	"	"	"	"
** Attitude Translation Command											
±X	"	"	"	"	"	"	"	"	"	"	"
±Y	"	"	"	"	"	"	"	"	"	"	"
±Z	"	"	"	"	"	"	"	"	"	"	"

TOTAL	DIG	DIS	ANALOG
Planetary	3	0	0
Earth Orbital	6	0	0

*These signals are for TM only. The actual gimbal and RCS valve commands are shown in GN&C list.
**Earth Orbital missions only

Tape Recorder Signal Interface List (CCS Output)

Signal Name/Symbol	Source	Dest.	Type	Class	No. of Wires	Imped.	Voltage	Resolution	No. of Words	Sampling or Update Rate	GND/CCS Logic
Tape Recorder 1 Pwr On	CCS	Recorder	DIS	N Comd	One	TBD	28V	NA	NA	Once	GND
Tape Recorder 2 Pwr On	"	"	"	"	"	"	"	"	"	"	"
Tape Recorder 1 Standby/Stop	"	"	"	"	"	"	"	"	"	2/Hour	CCS
Tape Recorder 2 Standby/Stop	"	"	"	"	"	"	"	"	"	"	"
Tape Recorder 1 Record	"	"	"	"	"	"	"	"	"	"	"
Tape Recorder 2 Record	"	"	"	"	"	"	"	"	"	"	"
Tape Recorder 1 Playback	"	"	"	"	"	"	"	"	"	2/Hr for 8 HR/WK	*GND/CCS
Tape Recorder 2 Playback	"	"	"	"	"	"	"	"	"	"	"
Tape Recorder 1 Rewind	"	"	"	"	"	"	"	"	"	**1/Week ***1/Day	GND
Tape Recorder 2 Rewind	"	"	"	"	"	"	"	"	"	"	"
Tape Recorder 1 Pwr Off	"	"	"	"	"	"	"	"	"	Once	CCS
Tape Recorder 2 Pwr Off	"	"	"	"	"	"	"	"	"	"	"

	DIG	DIS	ANALOG
TOTAL	0	12	0

*Ground commands initiate 1st playback command, CCS controls subsequent commands until all data is telemetered.
**Planetary missions only
***Earth Orbital missions only

Tape Recorder Signal Interface List (CCS Input)

Signal Name/Symbol	Source	Dest.	Type	Class	No. of Wires	Imped.	Voltage	Resolu-tion	No. of Words	Sampling or Update Rate	GND/CCS Logic
Tape Rec 1 Servo Phase	Recorder	CCS	A	TM	Two	TBD	TBD	1%	NA	2/Hour	NA
Tape Rec 2 Servo Phase	"	"	A	"	"	"	"	"	"	"	"
Tape Rec 1 End of Tape	"	"	DIS*	Control	One	"	"	NA	"	1/50 DAYS	"
Tape Rec 2 End of Tape	"	"	" *	"	"	"	"	"	"	"	"
Tape Rec 1 Beginning of Tape	"	"	" *	"	"	"	"	"	"	"	"
Tape Rec 2 Beginning of Tape	"	"	" *	"	"	"	"	"	"	"	"
Tape Rec 1 Temp	"	"	A	"	Two	"	"	0.3%	"	1/Min	"
Tape Rec 2 Temp	"	"	A	"	"	"	"	"	"	"	"
		DIG	DIS	ANALOG							
TOTAL		0	4	4							

*Logical 2V P-P

Solar Array Subsystem Signal Interface List (CCS Outputs)

Signal Name/Symbol	Source	Dest.	Type	Class	No. of Wires	Imped.	Voltage	Resolution	No. of Words	Sampling or Update Rate	GND/CCS Logic
SA A Containment Lid Released	CCS	SA	DIS	Cr Comd	One	10K Ω	28V	NA	NA	Once	GND
SA B Containment Lid Released	"	"	"	"	"	"	"	"	"	"	"
SA A Extend	"	"	DIS	"	"	"	"	NA	"	<40/Mission	"
SA B Extend	"	"	"	"	"	"	"	"	"	"	"
SA A Retract	"	"	"	"	"	"	"	"	"	"	"
SA B Retract	"	"	"	"	"	"	"	"	"	"	"
SA A Partial Retract/Extend	"	"	"	"	"	"	"	"	"	"	"
SA B Partial Retract/Extend	"	"	"	"	"	"	"	"	"	"	"
SA A Reconfigure	"	SA	"	"	"	"	"	"	"	Once	"
SA B Reconfigure	"	"	"	"	"	"	"	"	"	"	"
SA A Rotate CCW	"	Drive	DIG	"	"	"	"	8 Bits	One	1/Sec	CCS*
SA B Rotate CCW	"	"	"	"	"	"	"	"	"	"	"
SA A Rotate CW	"	"	"	"	"	"	"	"	"	"	"
SA B Rotate CW	"	"	"	"	"	"	"	"	"	"	"
		DIG	DIS	ANALOG							
TOTAL		4	10	0							

*Based on (1) closed loop control using sun sensor and (2) temperature bias on inbound missions.

Solar Array Subsystem Signal Interface List (CCS Inputs)

Signal Name/Symbol	Source	Dest.	Type	Class	No. of Wires	Imped.	Voltage	Resolution	No. of Words	Sampling or Update Rate	GND/CCS Logic
SA A Secured	SA Wing	CCS	DIS	Control	One	10K Ω	5V	NA	NA	1/Sec	NA
SA B Secured	"	"	"	"	"	"	"	"	"	"	"
SA A Not Secured	"	"	"	"	"	"	"	"	"	"	"
SA B Not Secured	"	"	"	"	"	"	"	"	"	"	"
SA A Containment Lid Not Released	"	"	"	"	"	"	28V	"	"	"	"
SA B Containment Lid Not Released	"	"	"	"	"	"	"	"	"	"	"
SA A Fully Deployed	"	"	"	Control	"	"	5V	"	"	"	"
SA B Fully Deployed	"	"	"	"	"	"	"	"	"	"	"
SA A Partially Deployed	"	"	"	"	"	"	"	"	"	"	"
SA B Partially Deployed	"	"	"	"	"	"	"	"	"	"	"
SA A Retracted	"	"	"	"	"	"	"	"	"	"	"
SA B Retracted	"	"	"	"	"	"	"	"	"	"	"
1) SA A Temp	"	"	A(41)*	"	Three	"	0-5V	5%	"	"	"
1) SA B Temp	"	"	A(41)*	"	"	"	"	"	"	"	"
2) SA A Voltage	"	"	A(41)*	"	Two	"	"	1%	"	"	"
2) SA B Voltage	"	"	A(41)*	"	"	"	"	1%	"	"	"
2) SA A Current	"	"	A(41)*	"	"	"	"	"	"	"	"
2) SA B Current	"	"	A(41)*	"	"	"	"	"	"	"	"
SA A Orientation Pos	Drive	CCS	A	Control	Four	20K Ω	0-5V	3%	NA	1/Sec	NA
SA B Orientation Pos	"	"	"	"	"	"	"	"	"	"	"
		DIG*	DIS	ANALOG							
TOTAL		2	12	2							

(1) Temp monitoring by CCS for biasing SA angle on inbound mission.
(2) For use in peak power tracking.

*Assume local A/D and multiplexing at SA resulting in 1 serial digital signal supplied to CCS from each solar wing.

Structures and Mechanisms Signal Interface List (CCS Outputs)

Signal Name/Symbol	Source	Dest.	Type	Class	No. of Wires	Imped.	Voltage	Resolution	No. of Words	Sampling or Update Rate	GND/CCS Logic
Truss Attach Pyro A Fire	CCS	S&M	DIS*	Cr Comd	One	560 Ω	28V	NA	NA	10/Sec	CCS
Truss Attach Pyro B Fire	"	"	"	"	"	"	"	"	"	"	"
Truss Rotate Pyro A	"	"	"	"	"	"	"	"	"	"	"
Truss Rotate Pyro B	"	"	"	"	"	"	"	"	"	"	"
Base Support Pyro A Fire	"	"	"	"	"	"	"	"	"	"	"
Base Support Pyro B Fire	"	"	"	"	"	"	"	"	"	"	"
** HGA Pyro A Fire	"	"	"	"	"	"	"	"	"	"	"
** HGA Pyro B Fire	"	"	"	"	"	"	"	"	"	"	"
Antenna Boom Attach Pyro A Fire	"	"	"	"	"	"	"	"	"	"	"
Antenna Boom Attach Pyro B Fire	"	"	"	"	"	"	"	"	"	"	"
SA Pkg Deploy Pyro A Fire	"	"	"	"	"	"	"	"	"	"	"
SA Pkg Deploy Pyro B Fire	"	"	"	"	"	"	"	"	"	"	"
Sunshade Release Pyro A Fire	"	"	"	"	"	"	"	"	"	"	"
Sunshade Release Pyro B Fire	"	"	"	"	"	"	"	"	"	"	"
Thruster Release Pyro A Fire	"	"	"	"	"	"	"	"	"	"	"
Thruster Release Pyro B Fire	"	"	"	"	"	"	"	"	"	"	"
** HGA Clock Angle	"	"	DIG	"	TBD	TBD	TBD	TBD	TBD	As Req'd	"
** HGA Cone Angle	"	"	"	"	"	"	"	"	"	"	"
Payload Release Pyro A Fire	"	"	DIS*	"	One	560 Ω	28V	NA	NA	10/Sec	GND
Payload Release Pyro B Fire	"	"	"	"	"	"	"	"	"	"	"
** Sci Pkg/Boom Pyro A Fire	"	"	"	"	"	"	"	"	"	"	"
** Sci Pkg/Boom Pyro B Fire	"	"	"	"	"	"	"	"	"	"	"
*** Retract SA Pkg A	"	"	DIS	"	"	"	"	"	"	"	"
*** Retract SA Pkg B	"	"	"	"	"	"	"	"	"	"	"

*50 - 100 ms pulse
**Planetary missions only
***Earth Orbital missions only

Signal Interface List

Signal Name/Symbol	Source	Dest.	Type	Class	No. of Wires	Imped.	Voltage	Resolution	No. of Words	Sampling or Update Rate	GND/CCS Logic
*** Docking Mechanism Latch	CCS	S&M	DIS	Cr Comd	One	560 Ω	28V	NA	NA	10/Sec	GND
*** Docking Mechanism Release	"	"	"	"	"	"	"	"	"	"	"
* Miscellaneous (50)	"	"	DIS(50)	"	"	"	"	"	"	1/Sec	"

TOTAL	DIG	DIS	ANALOG
Planetary	2	70	0
Earth Orbital	0	70	0

*Not specifically defined at this time.
***Earth Orbital missions only

Structures and Mechanisms Signal Interface List (CCS Inputs)

Signal Name/Symbol	Source	Dest.	Type	Class	No. of Wires	Imped.	Voltage	Resolution	No. of Words	Sampling or Update Rate	GND/CCS Logic
Truss Attach Pyro A Fired	S&M	CCS	DIS	Cr Comd	One	TBD	5V	NA	NA	1/Min	NA
Truss Attach Pyro B Fired	"	"	"	"	"	"	"	"	"	"	"
Truss Rotate Limit A	"	"	"	"	"	"	"	"	"	"	"
Truss Rotate Limit B	"	"	"	"	"	"	"	"	"	"	"
** HGA Clock Angle	"	"	DIG	"	"	"	"	0.1%	TBD	"	"
** HGA Cone Angle	"	"	"	"	"	"	"	"	"	"	"
SA Pkg Deploy Pyro A Fired	"	"	DIS	"	"	"	"	"	"	"	"
SA Pkg Deploy Pyro B Fired	"	"	"	"	"	"	"	"	"	"	"
SA Pkg A Deployed	"	"	"	"	"	"	"	"	"	"	"
SA Pkg B Deployed	"	"	"	"	"	"	"	"	"	"	"
* SA Pkg A Stowed	"	"	"	"	"	"	"	"	"	"	"
* SA Pkg B Stowed	"	"	"	"	"	"	"	"	"	"	"
Sunshade Release Pyro A Fired	"	"	"	"	"	"	"	"	"	"	"
Sunshade Release Pyro B Fired	"	"	"	"	"	"	"	"	"	"	"
Sunshade Deploy Verify	"	"	"	"	"	"	"	"	"	"	"
Thruster Release Pyro A Fired	"	"	"	"	"	"	"	"	"	"	"
Thruster Release Pyro B Fired	"	"	"	"	"	"	"	"	"	"	"
Thruster/Actuator Released	"	"	"	"	"	"	"	"	"	"	"
** Sci Pkg/Boom Pyro A Fired	"	"	"	"	"	"	"	"	"	"	"
** Sci Pkg/Boom Pyro B Fired	"	"	"	"	"	"	"	"	"	"	"
** Sci Pkg Stowed	"	"	"	"	"	"	"	"	"	"	"
* Docking Latch Verify A	"	"	"	"	"	"	"	"	"	"	"
* Docking Latch Verify B	"	"	"	"	"	"	"	"	"	"	"

*Earth Orbital Missions only
**Planetary mission only

Signal Interface List

Signal Name/Symbol	Source	Dest.	Type	Class	No. of Wires	Imped.	Voltage	Resolution	No. of Words	Sampling or Update Rate	GND/CCS Logic
** HGA Pyro A Fired	S&M	CCS	DIS	Cr Comd	TBD	TBD	5V	NA	NA	1/Min	NA
** HGA Pyro B Fired	"	"	"	"	"	"	"	"	"	"	"
** Antenna Boom Attach Pyro A Fired	"	"	"	"	"	"	"	"	"	"	"
** Antenna Boom Attach Pyro B Fired	"	"	"	"	"	"	"	"	"	"	"
** Antenna Boom Deploy Verify	"	"	"	"	"	"	"	"	"	"	"
Payload Release Pyro A Fired	"	"	"	"	"	"	"	"	"	"	"
Payload Release Pyro B Fired	"	"	"	"	"	"	"	"	"	"	"
Base Support Pyro A Fired	"	"	"	"	"	"	"	"	"	"	"
Base Support Pyro B Fired	"	"	"	"	"	"	"	"	"	"	"
Structural Strain Gauges	"	"	A(15)	TM	"	TBD	TBD	TBD	NA	1/Hour	"

TOTALS		DIG	DIS	ANALOG
	Planetary	2	26	15
	Earth Orbital	0	22	15

**Planetary mission only

Thermal Control Subsystem Signal Interface List

Signal Name/Symbol	Source	Dest.	Type	Class	No. of Wires	Imped.	Voltage	Resolution	No. of Words	Sampling or Update Rate	GND/CCS Logic

There are 43 to 46 heaters on-board SEPS. ON/OFF sequencing of these heaters is normally by thermostat control. Ground override commands are provided for contingency. These commands and temperature measurements appear in the particular subsystem that they are associated with. Potential heaters exist for the following:

Hg Feedline Heaters
Thruster Feedline Heaters
RCS Thruster Heaters
RCS Line Heaters
Sun Sensor Heaters
Star Tracker Heaters
*TV Camera Heaters
*Laser Radar Heaters
Battery Heaters

	DIG	DIS	ANALOG
TOTALS	0	0	0

*Earth Orbital missions only

PDS Signal Interface List (CCS Outputs)[3]

Signal Name/Symbol	Source	Dest.	Type	Class	No. of Wires	Imped.	Voltage	Resolution	No. of Words	Sampling or Update Rate	GND/CCS Logic
Umbilical A On/Off	CCS	PDS	DIS[1]	Cr Comd	One	560 Ω	28V	NA	NA	1/Min	GND
Umbilical B On/Off	"	"	"	"	"	"	"	"	"	"	"
Regulator A On/Off	"	"	"	"	"	"	"	"	"	"	CCS
Regulator B On/Off	"	"	"	"	"	"	"	"	"	"	"
Regulator Standby On/Off	"	"	"	"	"	"	"	"	"	"	"
Converter On/Off	"	"	"	"	"	"	"	"	"	"	"
Converter Standby On/Off	"	"	"	"	"	"	"	"	"	"	"
Inverter A On/Off	"	"	"	"	"	"	"	"	"	"	"
Inverter B On/Off	"	"	"	"	"	"	"	"	"	"	"
Battery Charge A On/Off	"	"	"	"	"	"	"	"	"	"	"
Battery Charge B On/Off	"	"	"	"	"	"	"	"	"	"	"
Battery Charge A Hi/Low	"	"	"	"	"	"	"	"	"	"	"
Battery Charge B Hi/Low	"	"	"	"	"	"	"	"	"	"	"
Low Volt Cutoff A On/Off	"	"	"	"	"	"	"	"	"	1/Min	CCS
Low Volt Cutoff B On/Off	"	"	"	"	"	"	"	"	"	"	"
Safe/Arm A On/Off	"	"	"	"	"	"	"	"	"	10/Sec	"
Safe/Arm B On/Off	"	"	"	"	"	"	"	"	"	"	"
Keep Alive Only On/Off	"	"	"	"	"	"	"	"	"	1/Min	"
PPU Converter On/Off	"	"	"	"	"	"	"	"	"	"	"
	DIG	DIS	ANALOG								
TOTAL	0	18	0								

(1) 50-100 msec pulse
(2) Additional component on/off commands/measurements are contained in the various other subsystems.

PDS Signal Interface List (CCS Inputs)

Signal Name/Symbol	Source	Dest.	Type	Class	No. of Wires	Imped.	Voltage	Resolu-tion	No. of Words	Sampling or Update Rate	GND/CCS Logic
Umbilical A On/Off	PDS	CCS	DIS	Control	One	TBD	28V	NA	NA	1/Min	NA
Umbilical B On/Off	"	"	"	"	"	"	"	"	"	"	"
Regulator A On/Off	"	"	"	"	"	"	"	"	"	"	"
Regulator B On/Off	"	"	"	"	"	"	"	"	"	"	"
Regulator Standby On/Off	"	"	"	"	"	"	"	"	"	"	"
Converter On/Off	"	"	"	"	"	"	"	"	"	"	"
Converter Standby On/Off	"	"	"	"	"	"	"	"	"	"	"
Inverter A On/Off	"	"	"	"	"	"	"	"	"	"	"
Inverter B On/Off	"	"	"	"	"	"	"	"	"	"	"
Battery Charge A On/Off	"	"	"	"	"	"	"	"	"	"	"
Battery Charge B On/Off	"	"	"	"	"	"	"	"	"	"	"
Battery Charge A Hi/Low	"	"	"	"	"	"	"	"	"	"	"
Battery Charge B Hi/Lo	"	"	"	"	"	"	"	"	"	"	"
Low Volt Cutoff A On/Off	"	"	"	"	"	"	"	"	"	"	"
Low Volt Cutoff B On/Off	"	"	"	"	"	"	"	"	"	"	"
Safe/Arm A On/Off	"	"	"	"	"	"	"	"	"	10/Sec	"
Safe/Arm B On/Off	"	"	"	"	"	"	"	"	"	"	"
Keep Alive Only On/Off	"	"	"	"	"	"	"	"	"	1/Min	"
PPU Converter On/Off	"	"	"	"	"	"	"	"	"	"	"
SA Wing A Current	"	"	A	Control	Two	TBD	TBD	1%	"	TBD	"
SA Wing B Current	"	"	A	"	"	"	"	"	"	"	"
Power Cond Current	"	"	A	"	"	"	"	"	"	"	"
SA Voltage	"	"	A	"	"	"	"	"	"	"	"
Converter Output Current	"	"	A	"	"	"	"	"	"	"	"
Converter Standby Current	"	"	A	"	"	"	"	"	"	"	"
DC Bus Voltage	"	"	A	"	"	"	"	"	"	"	"

Signal Interface List

Signal Name/Symbol	Source	Dest.	Type	Class	No. of Wires	Imped.	Voltage	Resolu-tion	No. of Words	Sampling or Update Rate	GND/CCS Logic
Battery Bus A Voltage	PDS	CCS	A	Control	Two	TBD	TBD	1%	NA	TBD	NA
Battery Bus B Voltage	"	"	A	"	"	"	"	"	"	"	"
Battery Cell A1 Voltage	"	"	"	"	"	"	"	"	"	"	"
Battery Cell A2 Voltage	"	"	"	"	"	"	"	"	"	"	"
Battery Cell A3 Voltage	"	"	"	"	"	"	"	"	"	"	"
Battery Cell A4 Voltage	"	"	"	"	"	"	"	"	"	"	"
Battery A Watthours	"	"	"	"	"	"	"	TBD	"	"	"
Battery B Watthours	"	"	"	"	"	"	"	TBD	"	"	"
Battery A Current	"	"	"	"	"	"	"	1%	"	"	"
Battery B Current	"	"	"	"	"	"	"	"	"	"	"
Battery Cell B1 Voltage	"	"	"	"	"	"	"	"	"	"	"
Battery Cell B2 Voltage	"	"	"	"	"	"	"	"	"	"	"
Battery Cell B3 Voltage	"	"	"	"	"	"	"	"	"	"	"
Battery Cell B4 Voltage	"	"	"	"	"	"	"	"	"	"	"
AC Bus A Voltage	"	"	"	"	"	"	"	2%	"	"	"
AC Bus B Voltage	"	"	"	"	"	"	"	"	"	"	"
AC Bus A Current	"	"	"	"	"	"	"	"	"	"	"
AC Bus B Current	"	"	"	"	"	"	"	"	"	"	"
Battery A Temp	"	"	"	"	"	"	"	1%	"	"	"
Battery B Temp	"	"	"	"	"	"	"	"	"	"	"

	DIG	DIS	ANALOG
TOTAL	0	19	27

Attached Science Package (Typical) Signal Interface List (CCS Outputs)*

Signal Name/Symbol	Source	Dest.	Type	Class	No. of Wires	Imped.	Voltage	Resolu-tion	No. of Words	Sampling or Update Rate	GND/CCS Logic
Scan Pltf Control:											
Arm Deploy	CCS	Pltf	DIS	TBD	One	TBD	TBD	NA	NA	Once	GND
Deploy	"	"	"	"	"	"	"	"	"	"	"
Remove Cover	"	"	"	"	"	"	"	"	"	"	"
Scan Control On	"	"	"	"	"	"	"	"	"	"	"
Scan Control Off	"	"	"	"	"	"	"	"	"	"	"
Cone Slew Positive	"	"	"	"	"	"	"	"	"	1/Sec	CCS
Cone Slew Negative	"	"	"	"	"	"	"	"	"	"	"
Clock Slew Positive	"	"	"	"	"	"	"	"	"	"	"
Clock Slew Negative	"	"	"	"	"	"	"	"	"	"	"
Fast Slew Rate	"	"	"	"	"	"	"	"	"	1/10 Sec	"
Slow Slew Rate	"	"	"	"	"	"	"	"	"	"	"
Narrow-Angle TV:**											
Start Frame	CCS	TV	DIS	"	One	"	"	"	NA	1/42 Sec	CCS
Start Scan	"	"	DIS	"	"	"	"	"	"	"	"
Calibrate	"	"	DIG	"	TBD	"	"	"	4 Bits	1/Hour	GND
Data Read	"	"	DIS	"	One	"	"	"	NA	1/42 Sec	CCS
Filter Wheel Advance	"	"	DIG	"	TBD	"	"	"	3 Bits	"	"
Beam Current Step	"	"	"	"	"	"	"	"	4 Bits	"	"
Exposure	"	"	"	"	"	"	"	"	6 Bits	"	"
Power On/Off	"	"	DIS	"	One	"	"	"	NA	<1/Hour	GND

*Planetary missions only
**Not on Out-of-Ecliptic mission

Signal Interface List

Signal Name/Symbol	Source	Dest.	Type	Class	No. of Wires	Imped.	Voltage	Resolution	No. of Words	Sampling or Update Rate	GND/CCS Logic
IR Radiometer:**											
Power On/Off	CCS	Radiom	DIS	TBD	One	TBD	TBD	NA	NA	<1/Day	GND
Mirror Advance	"	"	DIG	"	TBD	"	"	"	2 Bits	1/Sec	CCS
Channel Select	"	"	"	"	"	"	"	"	4 Bits	1/8 Sec	"
Gain Step	"	"	"	"	"	"	"	"	4 Bits	1/Hour	"
UV Spectrometer:**(b)											
Power On/Off	CCS	Spect	DIS	"	One	"	"	"	NA	<1/Day	GND
Calibrate On/Off	"	"	"	"	"	"	"	"	NA	1/Hour	"
Reset Mux	"	"	"	"	"	"	"	"	NA	1/Sec	CCS
Channel Select	"	"	DIG	"	TBD	"	"	"	4 Bits	1/10 Sec	"
Plasma Analyzer:											
Power On/Off	CCS	ANAL	DIS	"	One	"	"	"	NA	Once	GND
High Volt On/Off	"	"	"	"	"	"	"	"	"	"	"
Channel Sweep Start	"	"	"	"	"	"	"	"	"	10/Sec	CCS
Ion/Neutral Mass Spectrometer:**											
Power On/Off	CCS	Spect	DIS	"	One	"	"	"	NA	Once	GND
Ion Spectrum Scan	"	"	"	"	"	"	"	"	"	1/Sec	CCS
Neutral Spectrum Scan	"	"	"	"	"	"	"	"	"	"	"
Gain Step	"	"	DIG	"	TBD	"	"	"	4 Bits	10/Hour	"
Radar Altimeter:***											
Power On/Off	"	Radar	DIS	"	One	"	"	"	NA	Once	CCS
Gain Step	"	"	DIG	"	One	"	"	"	4 Bits	1/Hour	"

**Not on Out-of-Ecliptic mission
***Encke Rendezvous mission only
(b)On Out-of-Ecliptic mission replace by UV Photopolarimeter

Signal Interface List

Signal Name/Symbol	Source	Dest.	Type	Class	No. of Wires	Imped.	Voltage	Resolu-tion	No. of Words	Sampling or Update Rate	GND/CCS Logic
Meteoroid Impact Optical:											
Power On/Off	CCS	Sensor	DIS	TBD	One	TBD	TBD	NA	NA	Once	GND
High Volt On/Off	"	"	"	"	"	"	"	"	"	Once	"
Retarding Pot Anal:											
Power On/Off	CCS	Anal	DIS	"	One	"	"	"	NA	Once	"
Voltage Step	"	"	DIG	"	TBD	"	"	"	6 Bits	1/10 Sec	CCS
Plasma Wave Detector:											
Boom Deploy	CCS	Detector	DIS	"	One	"	"	"	NA	Once	GND
Sampling Rate	"	"	DIG	"	TBD	"	"	"	3 Bits	1/Hour	CCS
Waveform Capture Start	"	"	DIS	"	"	"	"	"	NA	Once	"
Elec Dipole Spec Scan	"	"	"	"	"	"	"	"	"	"	"
Search Coil Spec Scan	"	"	"	"	"	"	"	"	"	"	"
Loop Antenna Spec Scan	"	"	"	"	"	"	"	"	"	"	"
Waveform Read	"	"	"	"	"	"	"	"	"	1/10 Sec	"
Power On/Off	"	"	"	"	"	"	"	"	"	Once	GND
Magnetometer:											
Power On/Off	CCS	Mag	DIS	"	One	"	"	"	NA	Once	"
Bias SW Pos Advance	"	"	"	"	"	"	"	"	"	"	CCS
Bias Step X	"	"	DIG	"	TBD	"	"	"	2 Bits	1/Hour	CCS
Bias Step Y	"	"	"	"	"	"	"	"	"	"	"
Bias Step Z	"	"	"	"	"	"	"	"	"	"	"
Boom Deploy	"	"	DIS	"	One	"	"	"	NA	Once	GND
Sensor Select	"	"	DIG	"	TBD	"	"	"	2 Bits	<1/Day	"
		DIG	DIS	ANAL							
TOTAL		16	39	0							

Attached Science Package (Typical) Signal Interface List (CCS Inputs)*

Signal Name/Symbol	Source	Dest.	Type	Class	No. of Wires	Imped.	Voltage	Resolution	No. of Words	Sampling or Update Rate	GND/CCS Logic
Scan Pltf Control:											
Deployment Armed (2)	Pltf	CCS	DIS(2)	Control	Two	TBD	TBD	NA	NA	Once	NA
Boom Deployed	"	"	" (2)	TM	"	"	"	"	"	"	"
Cone Angle	"	"	DIG	Cont	TBD	"	"	0.1%	TBD	1/30 SEC	"
Clock Angle	"	"	"	"	"	"	"	"	"	"	"
Control Pwr On	"	"	DIS	TM	One	"	"	NA	NA	1/32 Min	"
Narrow-Angle TV:**											
Frame Count	TV	CCS	DIG	TM	TBD	"	"	Count	TBD	1/Min	"
Drift Rate	"	"	A	"	"	"	"	1.5%	NA	"	"
Line Count	"	"	DIG	"	"	"	"	Count	TBD	"	"
Light Level	"	"	A	"	"	"	"	1%	NA	"	"
Filter Position	"	"	DIG	TM	"	"	"	Count	TBD	"	"
Beam Current	"	"	A		Two	"	"	1%	NA	"	"
Vidicon Temp	"	"	A	TM	"	"	"	"	"	"	"
Optics Temp	"	"	A	TM	"	"	"	"	"	"	"
Camera Id	"	"	DIG	Cont	TBD	"	"	TBD	TBD	"	"
Power On	"	"	DIS	TM	One	"	"	NA	NA	1/32 Min	"
IR Radiometer:**											
Mirror Position	Radiom	CCS	DIG	TM	TBD	"	"	Count	TBD	1/30 Sec	"
Channel No.	"	"	"	TM	"	"	"	Count	"	"	"
Detector Temp	"	"	A(2)	"	Four	"	"	0.1%	NA	1/Min	"
Detector Volt	"	"	A	"	Two	"	"	"	"	"	
Power On	"	"	DIS	TM	One	"	"	NA	"	1/32 Min	"

*Planetary missions only
**Not on Out-of-Ecliptic mission

Signal Interface List

Signal Name/Symbol	Source	Dest.	Type	Class	No. of Wires	Imped.	Voltage	Resolution	No. of Words	Sampling or Update Rate	GND/CCS Logic
UV Spectrometer:**(b)				TM							
Mux Step	Spec	CCS	DIG	TM	TBD	TBD	TBD	Count	TBD	1/30 Sec	NA
Detector Temp	"	"	A	"	Two	"	"	1%	NA	"	"
High Voltage	"	"	A	"	"	"	"	0.1%	"	"	"
Channel	"	"	DIG	TM	TBD	"	"	Count	TBD	"	"
Power On	"	"	DIS	TM	One	"	"	NA	NA	1/4 Min	"
Plasma Analyzer:											
Channel Step	ANAL	"	DIG (2)	Cont	TBD	"	"	Count	TBD	1/30 Sec	"
High Voltage	"	"	A	Cont	Two	"	"	0.1%	NA	"	"
Power On	"	"	DIS	TM	One	"	"	NA	"	1/32 Min	"
ION/Neutral Mass Spect:**											
Anode Voltage	Spect	"	A	TM	Two	"	"	1%	NA	1/30 Sec	"
Ionization Voltage	"	"	A	"	"	"	"	1.5%	"	"	"
Gain Step	"	"	DIG	TM	TBD	"	"	Count	TBD	1/2 Min	"
Ion Current	"	"	A	"	Two	"	"	0.1%	NA	1/30 Sec	"
Power On	"	"	DIS	"	One	"	"	NA	"	1/32 Min	"
Meteoroid Impact Optical:											
Voltage	Sensor	"	A	TM	Two	"	"	1.5%	NA	1/2 Min	"
Power On	"	"	DIS	TM	One	"	"	NA	"	1/32 Min	"
Retarding Pot Anal:											
Voltage	ANAL	"	A	TM	Two	"	"	1%	NA	1/30 Sec	"
Negative Ion Current	"	"	A	"	"	"	"	"	"	"	"
Power On	"	"	DIS	TM	One	"	"	NA	"	1/4 Min	"
Radar Altimeter:***											
Power On	Radar	"	DIS	TM	"	"	"	NA	NA	Once	"
Gain Step	"	"	DIG	TM	"	"	"	Count	One	1/Hour	"
High Voltage	"	"	A	Control	Two	"	"	1%	NA	"	"

**Not on Out-of-Ecliptic mission
***Encke Rendezvous mission only
(b)On Out-of-Ecliptic mission replace by UV Photopolarimeter

Signal Interface List

Signal Name/Symbol	Source	Dest.	Type	Class	No. of Wires	Imped.	Voltage	Resolution	No. of Words	Sampling or Update Rate	GND/CCS Logic
Plasma Wave Detector:											
Boom Deployed	Detector	CCS	DIS	TM	One	TBD	TBD	NA	NA	Once	NA
Sampling Rate	"	"	DIG	"	TBD	"	"	Count	TBD	1/4 Min	"
Waveform Capture Stopped	"	"	DIS	"	One	"	"	NA	NA	1/30 Sec	"
Spacecraft Potential	"	"	A	"	Two	"	"	0.1%	"	"	"
DC Magnetic Field	"	"	A	"	Two	"	"	0.1%	"	"	"
Voltage	"	"	A(3)	"	Six	"	"	1%	"	"	"
Power On	"	"	DIS	TM	One	"	"	NA	"	1/4 Min	"
Magnetometer:											
Boom Deployed	MAG	"	DIS	"	One	"	"	NA	NA	Once	"
Bias SW Position	"	"	DIG(3)	Control	TBD	"	"	Count	TBD	1/30 Sec	"
Bias Voltage	"	"	A(3)	TM	Six	"	"	1%	NA	"	"
Null Current	"	"	A(3)	"	Six	"	"	"	"	"	"
Sensor Select	"	"	DIG	"	TBD	"	"	Count	TBD	"	"
Power On	"	"	DIS	TM	One	"	"	NA	NA	1/32 Min	"
			DIG	DIS	ANALOG						
TOTAL			19	18	29						

APPENDIX B

SEPS DETAILED SOFTWARE SIZING

SEPS PLANETARY MISSION

DETAILED SOFTWARE SIZING

SUBSYSTEM/FUNCTION	INSTRUCTIONS (16-BITS)	DATA (16-BITS)	TOTAL (16-BITS)	MAX EXECUTION RATE	SPEED (KAPS)
EXECUTIVE					
Task Management	275	350	625	1/sec	0.28
Interrupt Processor	60	20	80	2/sec	0.12
Discrete Processor	170	80	250	1/sec	0.17
I/O Supervisor	120	40	160	1/sec	0.12
Power Up Initialization	190	70	260	N/A	----
Math Utility Routines	300	0	300	1/10 sec	0.03
Common Data	0	500	500	N/A	----
PROPULSION					
Initialization	126	16	142	1/sec	0.13
PPU/Thruster On/Off Sequence	276	100	376	1/sec	0.28
Performance Monitoring	306	56	362	1/sec	0.31
Thrust Level Control	156	36	192	1/hr	----
Configuration/Reconfiguration	204	50	254	1/sec	0.20
Propellant Management	135	15	150	1/hr	----
ATTITUDE CONTROL					
Inertial Attitude Reference	342	110	452	1/sec	0.34
Initialization/Reinitialization	55	10	65	1/sec	0.06
Star Tracker Processing	374	70	444	1/min	0.01
Attitude Update	402	240	642	1/min	0.01
TVC/RCS Processing	390	173	563	1/sec	0.39
Solar Array Orientation	100	40	140	1/min	----
Mode Control	150	27	177	1/min	----

SUBSYSTEM/FUNCTION	INSTRUCTIONS (16-BITS)	DATA (16-BITS)	TOTAL (16-BITS)	MAX EXECUTION RATE	SPEED (KAPS)
GUIDANCE AND NAVIGATION					
Midcourse Guidance	0	70	70	1/10 sec	----
Approach Guidance	30	10	40	1/sec	0.03
DATA HANDLING					
Telemetry Processing	100	592	692	1/sec	0.10
Data Storage Management	40	10	50	1/sec	0.04
COMMUNICATIONS					
Antenna Pointing and Control	149	31	180	1/sec	0.15
Command Processing	1300	374	1674	1/4 sec	0.32
Mode Control	70	10	80	1/min	----
SOLAR ARRAY					
Length Control	75	15	90	1/sec	0.08
Peak Power Computation	75	15	90	1/sec	0.07
POWER DISTRIBUTION					
Equipment Control	150	200	350	1/sec	0.15

SUBSYSTEM/FUNCTION	INSTRUCTIONS (16-BITS)	DATA (16-BITS)	TOTAL (16-BITS)	MAX EXECUTION RATE	SPEED (KAPS)
MECHANISMS					
Antenna Deployment	0	5	5	N/A	0
Solar Array Deployment	0	13	13	N/A	0
Other Mechanisms Seq.	0	17	17	N/A	0
Payload Sequencing	0	20	20	N/A	0
Miscellaneous	0	50	50	N/A	0
THERMAL					
		NO CCS LOGIC REQUIRED			
REDUNDANCY MANAGEMENT					
Attitude Control	300	152	452	1/sec	0.30
Guidance and Navigation	0	0	0	0	0
CCS/DHS	735	79	814	1/sec	0.73
Power Distribution	156	73	229	1/sec	0.16
Communications	51	51	102	1/10 sec	----
Propulsion		(SEE PROPULSION SUBSYSTEM SIZING)			
SCIENCE PACKAGE					
Instrumentation Control	150	50	200	1/10 sec	0.01
TOTAL			11352		4.59

SEPS EARTH ORBITAL MISSION

DETAILED SOFTWARE SIZING

SUBSYSTEM/FUNCTION	INSTRUCTIONS (16-BITS)	DATA (16-BITS)	TOTAL (16-BITS)	MAX EXECUTION RATE	SPEED (KAPS)
EXECUTIVE					
Task Management	275	350	625	1/sec	0.28
Interrupt Processor	60	20	80	2/sec	0.12
Discrete Processor	170	80	250	1/sec	0.17
I/O Supervisor	120	40	160	1/sec	0.12
Power Up Initialization	190	70	260	N/A	----
Math Utility Routines	300	0	300	1/10 sec	0.03
Common Data	0	500	500	N/A	----
PROPULSION					
Initialization	126	16	142	1/sec	0.13
PPU/Thruster On/Off Sequence	276	100	376	1/sec	0.28
Performance Monitoring	306	56	362	1/sec	0.31
Thrust Level Control	156	36	192	1/hr	----
Configuration/Reconfiguration	204	50	254	1/sec	0.20
Propellant Management	135	15	150	1/hr	----
ATTITUDE CONTROL					
Inertial Attitude Reference	342	110	452	1/sec	0.34
Initialization/Reinitialization	55	10	65	1/sec	0.06
Star Tracker Processing	374	220	594	1/min	0.01
Attitude Update	402	240	642	1/min	0.01
TVC/RCS Processing	430	188	618	1/sec	0.43
Solar Array Orientation	100	40	140	1/min	----
Mode Control	150	27	177	1/min	----

SUBSYSTEM/FUNCTION	INSTRUCTIONS (16-BITS)	DATA (16-BITS)	TOTAL (16-BITS)	MAX EXECUTION RATE	SPEED (KAPS)
GUIDANCE AND NAVIGATION					
LOW-AUTONOMY-BASELINE					
Mid-course Guidance	275	50	325	1/10 sec	0.03
State Propagation	900	100	1000	1/sec	0.90
Sun Direction Determination	240	27	267	1/min	----
Navigation Update	0	0	0	----	----
Target State Propagation	150	20	170	1/min	----
Laser Radar Processing	65	35	100	1/sec	0.06
Rendezvous Guidance	150	35	185	1/sec	0.15
Mode Control	40	10	50	1/min	----
HIGH-AUTONOMY-OPTIONAL					
Mid-course Guidance	6000	700	6700	1/10 sec	0.60
State Propagation	900	100	1000	1/sec	0.90
Sun Direction Determination	240	27	267	1/min	----
Navigation Update	1000	500	1500	1/hr	----
Target State Propagation	150	20	170	1/min	----
Laser Radar Processing	400	110	510	1/sec	0.40
Rendezvous Guidance	600	300	900	1/sec	0.60
Mode Control	40	10	50	1/min	----
DATA HANDLING					
Telemetry Processing	100	615	715	1/sec	0.10
Data Storage Management	40	10	50	1/sec	0.04

SUBSYSTEM/FUNCTION	INSTRUCTIONS (16-BITS)	DATE (16-BITS)	TOTAL (16-BITS)	MAX EXECUTION RATE	SPEED (KAPS)
COMMUNICATIONS					
Low Gain Antenna Switch	14	3	17	N/A	----
Command Processing	980	309	1289	1/4 sec	0.24
Mode Control	70	10	80	1/min	----
SOLAR ARRAY					
Length Control	75	15	90	1/sec	0.08
Peak Power Computation	75	15	90	1/sec	0.07
POWER DISTRIBUTION					
Equipment Control	150	200	350	1/sec	0.15
MECHANISMS					
Solar Array Deployment	0	13	13	N/A	0
Other Mechanisms Sequencing	0	17	17	N/A	0
Payload Sequencing	0	20	20	N/A	0
Miscellaneous	0	75	75	N/A	0
THERMAL					

NO CCS LOGIC REQUIRED

SUBSYSTEM/FUNCTION	INSTRUCTIONS (16-BITS)	DATA (16-BITS)	TOTAL (16-BITS)	MAX EXECUTION RATE	SPEED (KAPS)
REDUNDANCY MANAGEMENT					
Attitude Control	300	152	452	1/sec	0.30
Guidance and Navigation	100	50	150	1/sec	0.10
	(400)	(200)	(600)		(0.40)
CCS/DHS	735	79	814	1/sec	0.73
Power Distribution	166	73	229	1/sec	0.16
Communications	51	51	102	1/10 sec	-----
Propulsion	(SEE PROPULSION SUBSYSTEM SIZING)				
TOTAL			12989		5.60
			(22439)		(7.26)

( ) - High-autonomy G&N (optional)

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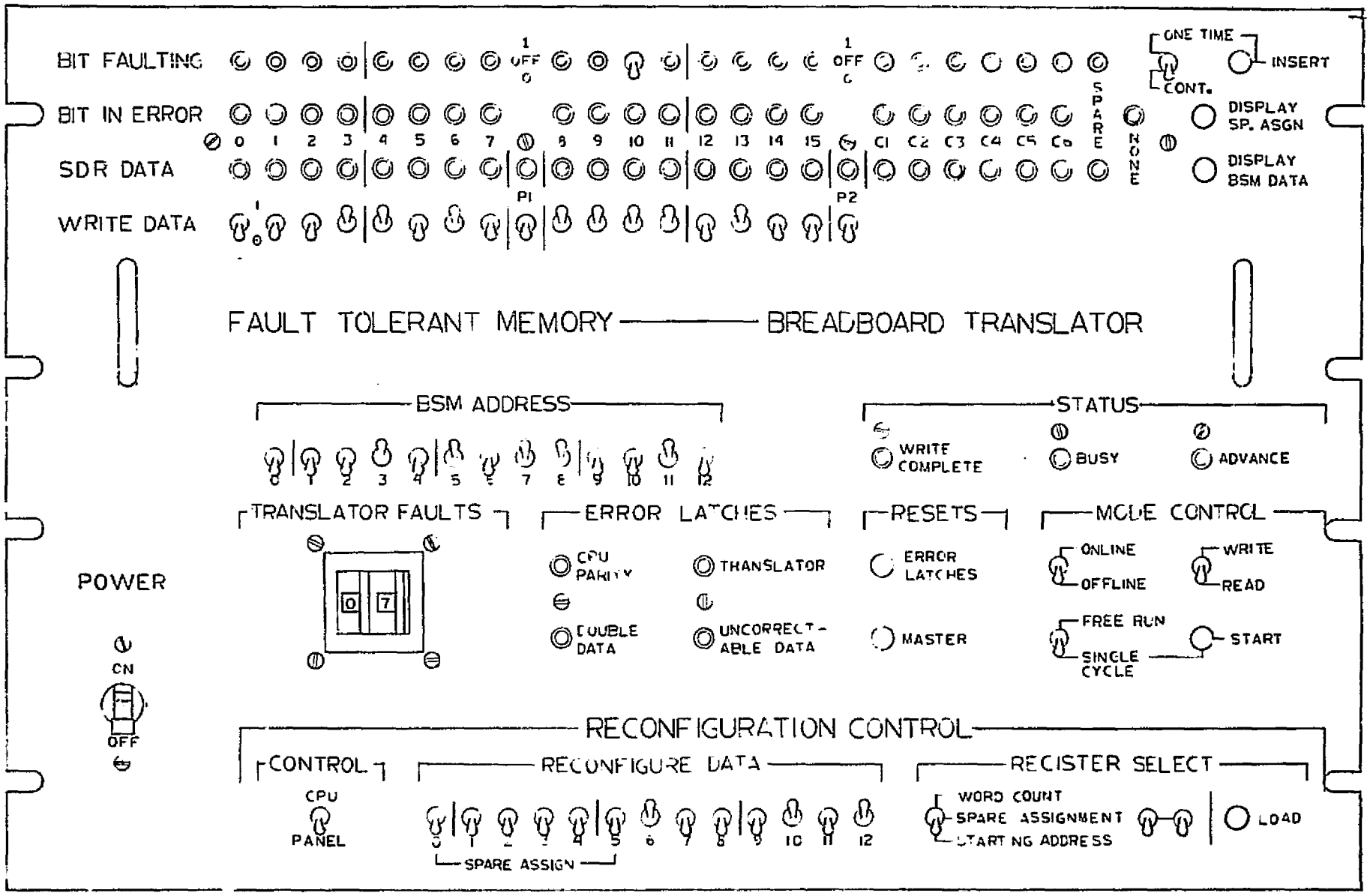
APPENDIX C

THE FAULT-TOLERANT MEMORY BREADBOARD



THE FAULT-TOLERANT MEMORY BREADBOARD PANEL LAYOUT

APPENDIX C

THE FAULT TOLERANT MEMORY BREADBOARD

1.0 INTRODUCTION

The fault tolerant memory breadboard design was accomplished under Technical Directive No. 28, Contract No. NAS8-20899. The design effort included the system design and LSI chip design for a system to be flight packaged, together with the design effort for the breadboard which functionally emulates the flight system. That design was carried through fabrication, checkout and demonstration to the C.O.R. under this contract number. The F.T.M. is the most critical of the functional elements which have been described in this document as being mandatory to satisfying the SEPS reliability requirements. Shown in Page C-2 is the Breadboard Panel Layout which shows the versatility in exercising fault injection and fault correction. The purpose of the breadboard is to demonstrate the error correction and detection capabilities of the system and the fault secure properties of the logic design. The principles of operation of the breadboard are explained in a paper entitled A MEMORY SYSTEM DESIGN WHICH CAN TOLERATE MULTIPLE STORAGE ARRAY FAULTS which is included and forms a part of this appendix.

2.0 PHYSICAL DESCRIPTION

The logic portion of the breadboard is implemented in commercially available TTL packages. These are mounted on an EECO plane with solderless wrapped interconnections. Also contained on the plane are receptacles which accept three memory cards each organized as 8192 X 9 bit arrays. The storage cards contain necessary support drivers as well as address decoding. The cards are standard IBM commercial technology and contain the same monolithic LSI storage chips as will be used in the flight system.

The EECO plane containing the circuitry is mounted on drawer slides and contained in an OPTIMA housing. A display and control panel is also mounted rigidly to the drawer slides. Access to the plane is obtained by sliding the front panel and plane out of the housing. Access to both the top and the bottom of the plane and to the front and the back of the control/display panel are thus obtained. Cabling to the assembly is sufficiently long and flexible that the assembly may be removed entirely from the housing and still operate.

Three regulated voltage supplies are mounted to the floor of the cabinet. A fan which circulates cooling air to the plane is mounted on the rear of the drawer. A suitable opening at the rear of the cabinet provides the air intake and a perforated top allows venting of the exhaust air.

3.0 OPERATIONAL DESCRIPTION

The breadboard is primarily a manually operated system having no associated processor. Provisions have been included within the design for expansion to a configuration utilizing the breadboard as a fault tolerant portion of a CPU memory. Under this expanded version, the CPU would also serve as the system controller via the I/O interface. The operation of the breadboard is controlled through the mode control switches whose basic functions will be described.

Reference the Fault-Tolerant Memory Panel Layout

ONLINE-OFFLINE - The online position of this switch is presently inoperable but would be used to transfer control and data lines to the memory port of the Hybrid Technology Computer (HTC). In the online position the breadboard would function as an 8K halfword fault tolerant memory. In the offline position, the switch causes the breadboard to be under manual control of the other mode switches.

SINGLE CYCLE-FREE RUN - The single cycle position of this switch is the normal setting. The free run position is provided for debug and causes the breadboard to perform memory cycles continuously at approximately 600 KHz. In the single cycle position, the breadboard will perform one memory cycle each time the START button is depressed.

START - Depression of this button causes the breadboard to perform one memory cycle each time it is depressed if in the single cycle mode or initiates the free run mode.

READING and WRITING MEMORY - Any of the 8192 word addresses may be selected by setting the desired binary address in a group of thirteen 'BSM ADDRESS' switches. Binary data to be written into the selected address of memory is determined by the setting of a group of eighteen 'WRITE DATA' switches, sixteen data bits, and two parity bits (odd parity).

With the READ/WRITE panel toggle switch set to write, depression of the start switch will cause the parity encoded word to be parity checked. If parity is incorrect a 'CPU Parity' light comes on and the write cycle is converted to a read of the same address. If the parity is correct six check bits are generated, checked, and stored along with the sixteen data bits in the selected memory address. The byte parity bits are not stored.

Read operations are performed by setting the address switches to the binary address of the selected word, setting the read/write mode control switch to 'READ', and depressing the start button. The word from storage is transferred into the SDR and the

consistency of the data and check bits is determined in accordance with the error encoding. Concurrently, byte parity bits are generated. If the word contains no errors no error lights come on. However, if there is an error a single 'bit in error' light will come on at the location of the errant bit. In the event there is a double error a 'double data' error light will come on signaling the condition but there is no indication of the locations of the bits in error, however.

FAULT-INJECTION - Faults can be deliberately injected into the system by means of twenty-two 'BIT FAULTING' three position switches. In the 'OFF' (center) positon no fault is injected, the '1' position causes the corresponding bit location to be stuck-at-1 (s-a-1),and the '0' position causes the corresponding bit location to be stuck-at-0 (s-a-0). Thus none, any, or all bits of a word read can be faulted. This facility permits system behavior under multiple fault conditions to be readily observed.

In addition to simulating faults in the storage array, faults may be injected into the translator logic to simulate faults in it. This is done by means of two sixteen position wheel switches. The zero position of each switch injects no faults. The remaining fifteen positions on each switch inject faults as follows: *

Switch Position	Left Switch	Right Switch
0	No Fault	No Fault
1	Syndrome 1 partial	Syndrome 2 partial
2	Syndrome 3 partial	Syndrome 4 partial
3	Syndrome 5 partial	Syndrome 6 partial
4	Syndrome 2 combined	Syndrome 1 combined

* Refer to Figure 4 of the paper for a description of partial and combined syndrome outputs, and to Figure 7 of the paper for descriptions of the other signal parts.

Switch Position	Left Switch	Right Switch
5	Syndrome 4 combined	Syndrome 3 combined
6	Syndrome 6 combined	Syndrome 5 combined
7	Syndrome P combined	Syndrome R combined
8	Syndrome Q combined	Syndrome S combined
9	PRS Parity	T XOR R
10	Spare	Spare
11	Spare	Error Analysis RCCO
12	Spare	Error Analysis Parity
13	Spare	Super Parity
14	Spare	Fail Corrector
15	Spare	Spare

With the exception of the right switch position 14 the above fault injection is done by inverting the signal on the line where the fault is injected. Since the dynamically self-checking circuitry in the translator has both 0's and 1's on the lines during normal operation, it is necessary to invert whichever value happens to be present at the time of fault-injection in order to simulate faulty line values.

RECONFIGURATION - The breadboard provides for functionally replacing any one of the twenty-two normal bit planes with a spare bit plane. To be effective the appropriate correct information must be written into this spare bit plane. The procedure for loading good information into the spare is to read each word including the bit from the bit plane to be replaced, correcting the error if present with the hardware; then storing the word at the same address but writing the correct bit into the spare bit plane as well as the bit plane being replaced. This procedure is done once for each word address, and when all word addresses have been restored, the spare bit plane will contain all correct bits. Provision is made in the breadboard for performing

this reconfiguration sequence automatically, on all or any selected portion of the memory by means of the group of reconfiguration control switches. The CPU/Panel switch is set to "PANEL'. Three registers must be loaded for reconfiguration selected by the 'REGISTER SELECT' switch. The word to be set in these registers are set in the 'RECONFIGURE DATA' switches. All thirteen switches are used for 'WORD COUNT' and 'STARTING ADDRESS', but only six (0-5) are needed for 'SPARE ASSIGNMENT'. The binary number representation is used for word count and starting address. The spare assignment code is the code utilized in the parity check matrix described in the paper included in this Appendix. Starting address and spare assignment are loaded first and word count LAST. The reason for this is that reconfiguration begins immediately upon loading the word count.

Since there is circuitry in the breadboard for only one spare bit plane, spare selection is not necessary; however, a pair of register select switches, now ineffective, are on the panel in the event that multiple (up to four) spares capability should ever be added.

There is a group of three 'STATUS' lights: 'WRITE COMPLETE' is lighted after a write cycle is completed and is turned off when a new cycle is begun. BUSY and ADVANCE are illuminated while a memory cycle is in process.

A 'DISPLAY SP. ASGN' button causes the light in the 'BIT IN ERROR' row to be lighted at the position to which the spare bit plane is assigned. The 'DISPLAY BSM DATA' button, when depressed, causes the 'SDR DATA' row of lights to display the input to the SDR rather than the contents of the SDR.

There are two 'RESETS' buttons. The one labeled 'ERROR LATCHES' resets only the four error latches. The one labeled 'MASTER' resets the entire system.

4.0 Conclusions

The original purpose for the breadboard was to verify the design approach for the fault tolerant memory system. All aspects operate as designed. Faults may be injected at will. All single bit errors may be detected, located, and corrected. All double errors are detected. Faults injected into the translator circuitry are detected on the first operation. Partial and total reconfigurations operate as designed, and the original BSM is kept current along with the assigned spare bit plane. Thus all features of the design operate as intended.

The breadboard will be a useful tool in the development of reconfiguration strategies. The criteria for initiating reconfiguration has not been determined. Clearly, a log of errors encountered - their bit position and address location would be useful for determining system status. Reconfiguration should be deferred until it is determined that there is a systematic fault in a bit plane which causes many errors in that bit plane. It has been calculated that an average of 92 random errors would be expected in an 8192 word memory before a double error was encountered. Thus reconfiguring each time an error is encountered is not an efficient strategy.

A MEMORY SYSTEM DESIGN WHICH CAN TOLERATE MULTIPLE STORAGE ARRAY FAULTS*

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ABSTRACT

The memory portion of an aerospace digital computer is typically much more prone to failure than the logical/control portion, because of the larger circuit count. Various approaches for tolerating one or more memory failures have been taken on past and current aerospace programs -- all dependent on massive replication to achieve the fault tolerance. The advent of monolithic random access storage arrays provides an efficient means of achieving acceptable reliability for the long term (e.g. 3 years) unmaintained space missions currently being planned. The approach involves encoding the stored words in an error correcting code (ECC) and organizing the storage array such that likely faults in the storage array manifest themselves as errors detectable and correctable by the ECC.

A fault tolerant memory system for aerospace applications is currently under development. Salient features of this system are:

- Storage redundancy at the bit plane level rather than at the whole array level.
- Completely self-checking, self-testing translator circuitry which utilizes the normal data flow to dynamically check the translator circuitry during normal operation.
- "Lookaside" correction which bypasses the correction circuitry timing delays if correction is unnecessary.
- Level merging of the translator data flow logic to minimize circuit delays.
- Code independent chip designs.
- Spare bit plane reconfiguration switching which enables up to four spare bit planes to replace any failed bit plane position.
- Recovery of all lost information from a bit plane failure by reading each address location, correcting the bit from failed bit plane if necessary, and storing the correct bit in the spare bit plane.
- Tolerance of up to five massive bit plane failures by virtue of the error correction code and four spare bit planes.

The storage array is to be comprised of basic memory modules, developed for the NASA SUMC Computer program. A breadboard demonstration model of the system has been assembled. It implements the storage array with the same storage chips that are used in the memory module. The translator logic is implemented in commercially available TTL logic. Extensive fault-injection capabilities are incorporated for verification of the system operation, performing experiments and developing reconfiguration criteria.

I. INTRODUCTION

Background

Memory is not only a critical functional part of any airborne or spaceborne computational system but is also a major programmatic concern to each developer and user. The reasons for this are perhaps obvious; for most airborne and space applications, a major portion of the cost, power, and weight can be attributed to memory; depending on the type of technology and the amount of memory employed, memory systems in the past have normally contributed between 65% to 85% of the failure rate of the entire computational system. Although cheap, low powered, and highly reliable operational semiconductor memories for airborne and space applications have been projected for several years, only recently have they begun to surface as viable flight options. During the last few years, discrete improvements in the development of large scale integrated (LSI) circuits applicable to the central processing unit (CPU) have made the ratio of memory to CPU failure rates even more unbalanced than it had previously been.

The National Aeronautics and Space Administration (NASA) has employed fault-tolerant memories for several years on numerous programs. The Launch Vehicle Digital Computer (LVDC) of the Saturn IB/V program which was developed in the early 1960's required duplexed memory modules utilizing parity checking and sense amplifier current monitoring to resolve conflicts in case of disagreement in the duplexed pair of modules. This approach reduced the failure rate of a simplex memory by a factor of approximately 25.

The computational system for the Skylab/Apollo Telescope Mount (ATM) utilized an entire computer system backup to the prime to provide the necessary reliability. The guidance, control, navigation and data management computational system for Space Shuttle utilizes both triple modular redundancy (TMR) and standby spares. Generally, in these systems massive redundancy was employed to obtain a small degree of fault-tolerance at the expense of increasing complexity, power, and weight by a factor greater than two. Future payloads such as Spacelab, the Large Space Telescope (LST), and Space Tug will undoubtedly require some form of memory error coding or redundancy because of either the long unmanned operating periods or the critical periods of operations where human life is in jeopardy. The Solar Electric Propulsion Stage (SEPS) is another application which requires the utilization of a long life (three years) memory system.

*The hardware design and implementation was supported by NASA Contracts NAS8-20899 and NAS8-30749

In the past, various techniques have been developed and utilized to provide some degree of memory failure detection, error correction, and system recovery, ranging from simple parity, through more sophisticated error coding schemes and organizations. Some rather sophisticated schemes have been described in the literature[1,2,3,4]. Many of the approaches used in the past such as duplexing and TMR, are extremely complex from a hardware implementation viewpoint and can tolerate only a single failure. Auburn University under contract NAS8-26930 to the Marshall Space Flight Center is assessing trade-offs in such parameters as reliability, fault tolerance, ecomplexity, power, weight, and coverage for various schemes which have been proposed. The concept of coverage [5,6] is a very important parameter in dealing with long life systems.

Features

Some of the salient features of a fault-tolerant memory system required for airborne and space applications are:

- o Memory organization to insure independent failure modes within the system.
- o Techniques which yield a high degree of system coverage.
- o Fault-tolerant schemes which can be implemented independent of the technology employed.
- o Techniques which are independent of system application i.e., can be used with either a simplex or redundant central processing unit.
- o High degree of fault-tolerance with minimum increase in complexity.
- o Minimum impact in memory operating speeds.

The fault-tolerant memory technique presented herein satisfies many of these features.

The circuitry which implements the error correcting encoding is called a translator because a code-to-code translation is done on every store and fetch operation. It is obvious that the translator is in a very strategic location relative to system operation. Undetected failures of the translator can invalidate the information upon which the system operates. For this reason, the circuitry of the translator is designed to be dynamically self-checking and self-testing. The self-checking feature detects the occurrence of any single component failure wherever it causes an erroneous result. The self-testing feature insures that every circuit is tested during normal operation.

This first section lays the foundation for the necessity of reliable memory systems in future space missions. The second section is an overall description of the system being implemented. A more detailed description of the LSI chips and their operating features together with an illustration of the dynamic checking is given in Section III. The experimental efforts involved with system verification and reconfiguration strategy development are covered in Section IV. Section V gives conclusions and acknowledgments.

II. MEMORY SYSTEM OVERVIEW

The memory system design to be described has been implemented in a breadboard system. The breadboard has extensive fault injection capabilities. Experiments with the breadboard are currently planned with the objective of determining preferred reconfiguration criteria.

The LSI chip designs are completed. Modules for packaging the chips were previously designed and are available. A flight package design of the system is currently underway--scheduled for completion in 1975 and for prototype build during 1976.

Fault Tolerant Memory Organization and Operation

Two major features distinguish this memory system from more conventional memory systems. The first feature is the organization of the array into independent single bit wide planes. Each bit plane has its own address decoding as well as read/write storage elements. The second feature is the addition of a unit called the translator. On store operations the translator receives information in byte parity encoded form from devices which utilize the memory and re-encodes the data with an error correction code for storage. On read operations the translator checks the consistency of the check and data bits of the word read from memory. In the event of an error, it locates the errant bit and inverts it, thus correcting the error. When a good set of data bits is determined, byte parity is generated by the translator for transmission to the requesting unit.

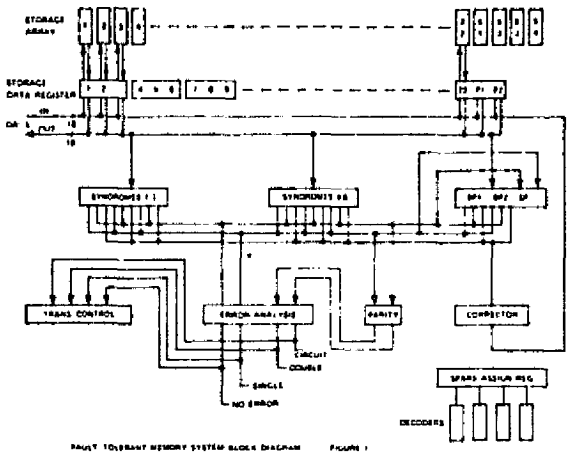
Spare bit planes are incorporated into the system. The combination of the independent array organization, the error correction encoding, and the translator correcting capabilities facilitates sparing at a bit plane level rather than at the whole array level. In the event of a bit plane failure, a spare bit plane may be substituted in the bad bit position. Recovery is effected by reading the successive address locations in the memory, correcting a bad bit if necessary, and restoring the corrected word in the same address location, thereby providing good information to the replacement spare bit plane.

There are four spare bit planes which enable up to five massive array failures to be tolerated. The storage array is comprised of basic memory modules (BMM's) which were developed for the NASA MSFC SUMC computer program. The BMM is organized as an 8K x 1 bit array with on the chip address decoding. There is at least one BMM for each bit of the storage word. There would be 22 basic storage modules in an 8K x 22 bit main store. Each bit plane would be comprised of one BMM. For a 16,384 word array each bit plane would contain two BMM's, etc.

The 22 bit word length in the system being designed is comprised of 16 data bits and 6 check bits to implement a modified Hamming type single error correct/double error detect code. This code was chosen because it is efficient in circuitry. It detects all single and double errors and has good multiple error detecting properties. The choice of the Hamming code and the single bit wide independent array organization are consistent since likely single failures will be detected and corrected by the code.

This code would not be effective if the plane width was greater than one bit because many likely failures could not be circumvented by the code.

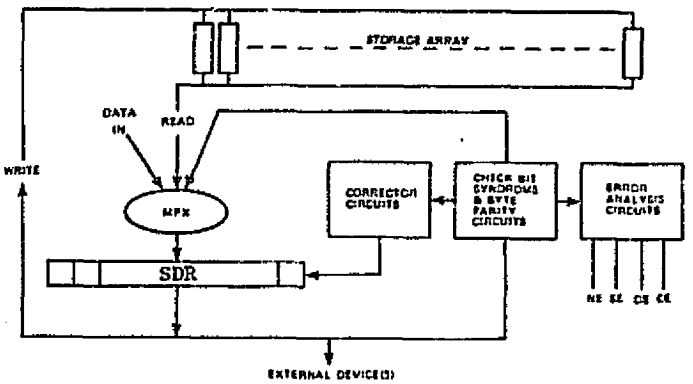
Figure 1 shows the overall organization and functional partitioning of the system. The bit planes of the storage array are shown at the top. With the exception of the storage array blocks, all other blocks in Figure 1 represent LSI TTL logic chips. There are six chip types represented, three of the types have multiple function usage within the system.



FAULT TOLERANT MEMORY SYSTEM BLOCK DIAGRAM FIGURE 1

Basic Translator Operation

Referring to Figure 2, the basic translator is partitioned into five major data flow areas: an input multiplexer, a storage data register (SDR), parity trees, error analysis, and corrector. The SDR is the major working register for the translator. All data inputs to be stored from external devices are read into the SDR and all data read from the storage array is read into the SDR. The Hamming encoded word read from main store is validity checked by the parity circuits (syndromes) and the error analysis circuits. In the event that there is no error detected, byte parity bits are generated and the word is transmitted to the requesting device. In the event there is a single error indicated by the error analysis, the syndrome pattern is decoded by the corrector. A correction signal is generated on the appropriate bit in error line to the SDR where the bit is inverted. The cycle of checking the validity is repeated and in the event that a correction was indeed made, the byte parity bits are generated and the word transmitted with the appropriate signal that a single error has occurred but was corrected.



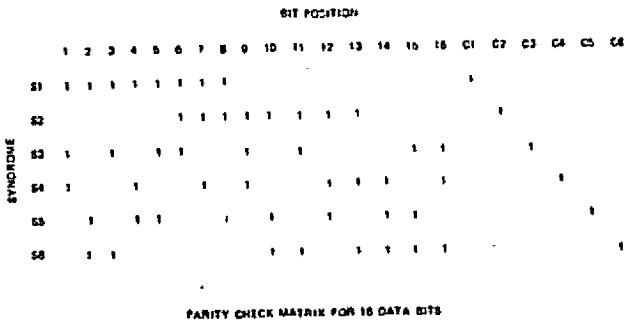
TRANSLATOR OPERATION

FIGURE 2

III. MEMORY SYSTEM IMPLEMENTATION FEATURES

The Parity Check Matrix

The translator design and operation follow closely the principles described in Reference [7]. The odd weight Hamming code is structured as described in Reference [8]. Let us consider first the parity check matrix of the Hamming code being used shown in Figure 3. There are 16 data bit position columns labeled 1 through 16. There are 6 check bit columns labeled C1-C6. Each check bit is generated to give odd parity over the field consisting of itself and 8 associated data bits in the same row of the matrix. Thus, C1 would be generated as 0 or 1 if data bits 1 through 8 had odd or even parity, respectively. Similarly, check bit 2 would be generated to give odd parity over the field consisting of itself and data bits 6 through 13. It should be noted that each column of the parity check matrix consists of an odd number of 1's. The data bit columns have three 1's and the check bit columns have a single 1. This is the reason the code is termed an odd weight code.



PARITY CHECK MATRIX FOR 16 DATA BITS

FIGURE 3

Error Detection and Location

On read operations, each of six fields, consisting of eight data bits and an associated check bit, is checked for odd parity. The parity indication signals generated for these six 9-bit fields are called syndromes labeled S1 - S6 in Figure 3. In the event that one or more syndromes indicate a discrepancy, an error is flagged. The pattern of the syndromes is analyzed to determine the type of error and, in the event of a single error, the syndrome pattern indicates the position of the errant bit.

Each data bit and each check bit has a unique pattern of 1's in its column. Thus, if data bit 1 was in error, then syndromes 1, 3, and 4 would indicate discrepancies. The combination of syndromes (1, 3, 4) uniquely identifying data bit 1 as the errant bit. In this way, the syndrome patterns are decoded to locate a single bit error.

Another feature of this odd weight code structure is that when an odd number of syndromes indicate a discrepancy there is a single correctable error and when an even number of syndromes indicate a discrepancy there is a double error. If a double error occurs the translator cannot correct the condition and the double error signal is used to disable the correction function and to alert the system control that the situation exists. In the parity check matrix there is a total of nine 1's in each row. This determines the maximum number of inputs to the parity trees which generate the syndromes.

The Parity Trees

The construction of the parity trees used in the translator augments the self-checking/self-testing properties of the translator. Figure 4 illustrates the organization for one of the three parity trees on a parity chip. There are nine input bits per tree and each tree is divided into a six bit section and a three bit section. There is a partial output for the six bit section of the tree and another for the three bit section. There is also a combined output which represents the parity over all nine input bits. The pair of partial outputs is called the 'morphic' output of the parity network while the combined output is the usual logical output.

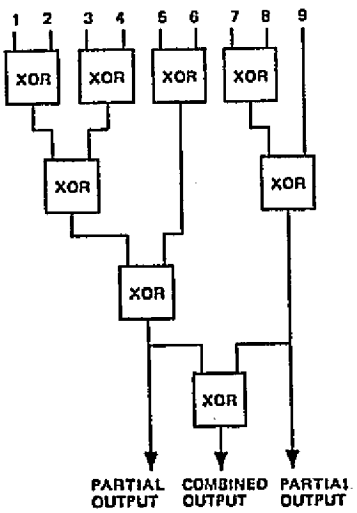


FIGURE 4. FUNCTIONAL PARITY TREE REPRESENTATION

The same physical parity tree is used for generating the check bits on store operations and generating the syndromes on read operations. Since odd parity is being used, an error free syndrome from the morphic output is indicated by a 01 or a 10 signal on read cycles. In the event of a fault within the parity tree network which results in an erroneous output, only one leg of the morphic output will be effected. Therefore, single gate failures in these circuits propagate to the output where they may be detected. Thus an odd parity input to a parity circuit, containing an error causing fault, will result in a 00 or 11 morphic output. Of course, an even parity input to a fault-free parity tree, will also cause the morphic output to be 00 or 11.

The Correction Decoder

The correction decoder illustrated in Figure 5 consists functionally of 27 six input AND gates which decode each of the 20 combinations of six things taken three at a time, the six combinations of six things taken one at a time, and the single combination of none of six. The outputs from the decoder are wired to the appropriate SDR bit positions. All twenty of the three of six combinations are available on the chip, however, only the appropriate 16 are utilized for the sixteen data bit positions in the code we have chosen. The inputs to the decoder are the combined outputs of the six syndrome parity trees.

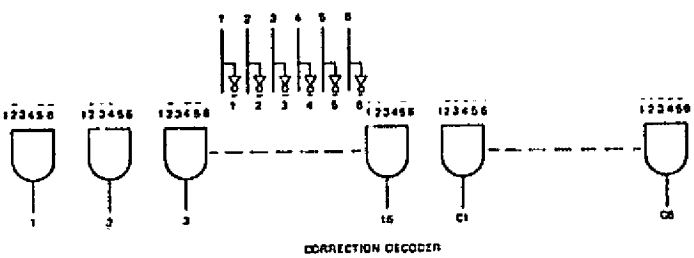
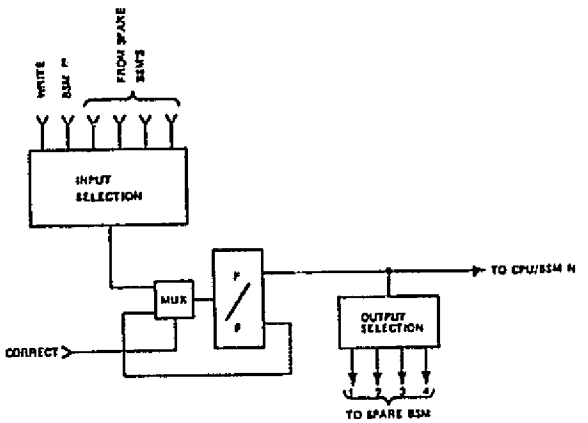


FIGURE 5

The Storage Data Register

Figure 6 is a functional illustration of one bit on the register chip. It is on this chip that the spare selection switching and the bit correction are effected. Each chip accommodates three such bits. The flip-flop register is labeled FF. The input to the flip-flop is from a two input multiplexer. The input to this multiplexer in turn is either from a selection multiplexer, or from the complement output of the flip-flop. When a correction to a bit in the register is to be made, the appropriate correction decoder position is selected which defines the bit position to be corrected. Each decoder output line is wired to a unique register bit position and is shown as the line labeled correct. This signal switches the input of the multiplexer from the normal spare selection multiplexer mode to the complement output of the flip-flop, and inverts the flip-flop.



REGISTER, SPARE SWITCHING, AND CORRECTION

FIGURE 8

The upper multiplexer normally controls the input to the flip-flop. As shown, the input may be from an external user device, or from the corresponding position bit plane, or from any one of the four spare bit planes. The output of the four spare bit planes are available to each bit position of the storage data register. Thus, a spare bit plane may be utilized for any bit position. The output of the flip-flop is available to the external user devices, to the write line of the associated position bit plane, to the spare bit planes, and to the remainder of the translator circuitry. In the event a spare bit plane has been selected for this particular bit position, the output demultiplexer directs the signal to the proper spare. Each of the four spares can receive bit input information from any one of the SDR bit positions. Thus, the SDR chips serve as the working register for the translator as well as the circuitry for correcting errant bits and spare reconfiguration switching. Note that the original bit plane assigned to a given position always has the current information written into it even though the output from a spare is being used for that particular bit position. The purpose of this is to maintain the bit plane current if possible, in the event that it is desirable to put it back on line at a future time.

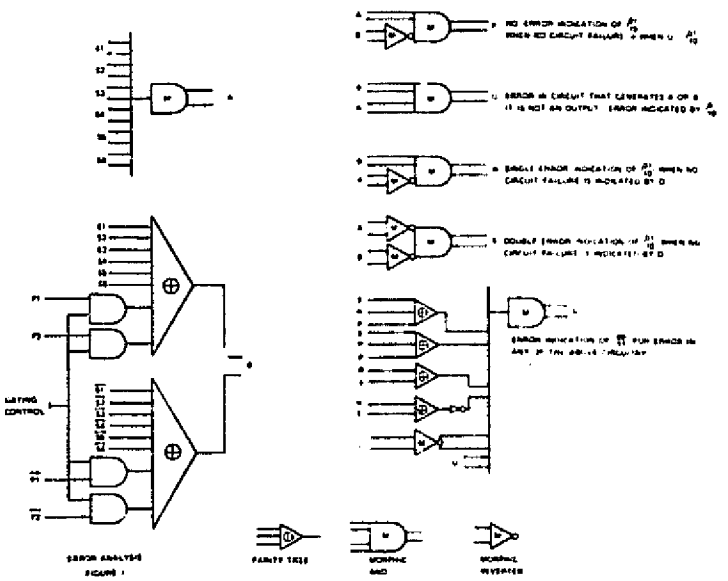
Morphic Logic

The error analysis portion of the translator is perhaps the most unique portion. It is implemented in morphic logic described in Reference 9. The morphic logic uses dual line pairs to replace the single lines in conventional logic. Morphic logic functions are composed of conventional logic gates arranged as two independent tree structures so that a fault of a single gate in the morphic logic propagates to the output where it can be detected. Circuits representing morphic invert, morphic AND, morphic OR, morphic exclusive-OR, etc., have been devised. Combinations of these morphic gates can be utilized to implement any logical function. The morphic logic equivalent of a conventional logic 1 is a 01 or a 10, $\begin{bmatrix}01\\10\end{bmatrix}$, on the line pair. The morphic logic equivalent of a conventional logic 0 is $\begin{bmatrix}00\\11\end{bmatrix}$ on the morphic line pair. For explanation of the error analysis circuits for this translator, the nomenclature $1_M \Leftrightarrow \begin{bmatrix}01\\10\end{bmatrix}$, and $0_M \Leftrightarrow \begin{bmatrix}00\\11\end{bmatrix}$ will be used.

Error Analysis of Word Read From Storage

The translator error analysis will be illustrated by explaining its operation for checking the word read from storage. The verification of byte parity checking and generation and check bit generation will then be explained.

The AND_M whose output is labeled A in Figure 7 has inputs from the morphic output of the syndrome generation parity trees S1 - S6. Since odd parity is used in the encoding, on read-out all of the syndrome partial signals should be 1_M if no error has occurred. Thus, the output A should be 1_M. Two parity trees are shown as the input B in Figure 7. There are an even number of syndromes (6). One each of the two morphic lines from each of the syndrome generators (the byte parity tree inputs are inhibited during read cycles) are inputs to the two parity trees whose outputs form B. Since the syndrome no error condition is 1_M and there are overall an even number of syndromes, there should be in total an even number of morphic (and logical) 1's under a no error condition. Since this is true, both parity trees should have like parity either odd or even since the sum of two odds or of two evens is even. The input B in Figure 6 should be 0_M under a no error condition. The AND_M gate whose output is P indicates NO ERROR as 1_M when the A and B signals are normal.



The AND_M gate whose output is Q indicates a translator circuit failure condition. There is no valid condition of the inputs which causes outputs A and B to be 1_M simultaneously. This condition is indicative of a failure in the circuits which generate A or B. Therefore, the AND_M gate whose output is Q senses this condition as a circuit error.

A single error is manifest as an odd number of 0_M syndromes -- one syndrome or three syndromes having a value of 0_M. Under this condition the output A will be a 0_M and the output B will be 1_M. The output A is inverted to make it a 1_M and combined with the output B which will be 1_M to cause signal R to be 1_M -- the single error condition signal.

The AND_M gate whose output is S senses a double error condition. The output A will be 0_M as will the output B in the presence of a double error in the word read from storage. Inversion of both these outputs makes them both 1_M and when combined in the AND_M gate, whose output is S, indicates the double error condition.

The AND_M whose output is D indicates a circuit error condition. The input U is for byte parity circuit checks. The signal Q (mentioned previously) is inverted because its normal (no error) indication is a 0_M. In order to maintain consistency all inputs to the AND_M should, under normal conditions, be 1_M's.

Therefore, the signal Q inverted is 1_M during normal operation. The signal T is used for checking the validity of the generated check bits on write operations and the validity of the generated byte parity bits on read operations. It is proved [7] that with the code structure herein utilized the parity of the byte parity bits and the parity of the code check bits should be the same; therefore, their combined parity should always be even. The signal T is the morphic output of a parity tree whose inputs are the two byte parity bits and the six combined outputs of the parity trees which generate the check bits.

The two parity trees with T and R inputs together with an inverter perform the logical operation T = R which is true when there is a valid single error condition and no circuit failures. Certain circuit failures might be detected as a single data error without this check.

A check is made to see that there is not an even number of the inputs P, R, and S in a 1_M state because P, R and S are mutually exclusive conditions. Should none or two of these three signals be up, there will be an even number of logical 1's which, distributed between the two parity trees whose inputs are PRS, will make their output 0_M. That is a failure indication causing the output D to be 0_M.

This discussion of the read cycle operation is intended to illustrate how the morphic logic is utilized to provide self-checking during normal operation. Since the normal data flow constantly changes, the translator circuits assume both states, which provides the self-testing property.

IV. EXPERIMENTAL SYSTEM

Purpose

An experimental breadboard of the memory system has been built. The breadboard has extensive fault injection and display circuitry incorporated under panel control. It implements the logic of the flight system described plus the necessary timing and control hardware which enables it to operate as a stand-alone memory system. Future plans include incorporating a SUMC computer in the breadboard.

A significant amount of simulation and analysis has been done to verify the fault security and the self checking properties of the design. The breadboard system will permit much more extensive verification and statistical quantification of these properties, especially under conditions where failures result in various combinations of faults and errors. When the SUMC computer is included in the breadboard it will be practical to systematically generate patterns in the memory and observe the dynamic behavior of the system and the inherent degree of independence the design possesses.

The extensive analysis is a prerequisite for developing effective reconfiguration strategies --when to switch in a spare, and when to tolerate some few words with correctable errors which occasionally require a lengthened access cycle. Of course, an optimum reconfiguration strategy is dependent on the application (the mission) as well as the behavioral properties of the system under various fault and error conditions.

Fault Injection

The experimental system has two types of fault injection: (a) The state of the line is at no fault, stuck-at-1, or stuck-at-0, and (b) The state of the line is either inverted (fault injected) or not inverted (no fault injected). The A type "stuck-at" faults are injected in each bit line of the array readout lines and each bit is individually selectable. The B-type invert faults are utilized throughout the translator logic. Each parity tree combined output and one leg of the morphic output are subject to inversion under panel control. Within the error analysis, one leg of each morphic block shown in Figure 7 may be inverted. Additionally, the correction decode circuits may be gated OFF to preclude making a correction in the presence of a single error.

The fault injection capabilities are believed to be adequate for duplicating virtually any condition it will be desired to study.

Other Features

The control panel displays by means of LED's, the bit(s) being faulted, the fault indication, and the error signals from the error analysis. In addition, there is control of single cycle or free run mode. Provision is made to select a spare bit plane and assign it to any bit position (reconfiguration) and to select a starting word address and select any number of successive storage addresses to be restored. Thus, partial or total refurbishing may be utilized during a recovery cycle.

CONCLUSIONS AND ACKNOWLEDGMENTS

The translator logic requires twenty chips. The system simulations indicate memory access times, without correction, to be of the order of three-fourths of a microsecond and one microsecond when correction is necessary. Loading a spare bit plane with good data could be done in less than two microseconds per storage location. The implementation and speed penalties are thus not severe. Future emphasis is to be on designing the flight package, designing a fault tolerant system control, and devising the algorithms which implement the switching strategies.

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